# FPGA Implementation of the Reconfigurable Control System for AC Drives Fed by Tandem Converter

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***Abstract - The paper focuses on the implementation in Field Programmable Gate Arrays (FPGA) of vector control systems of the induction motor supplied from the tandem (hybrid) static-frequency converter. Reconfigurable control structure ensures different strategies for operating modes with non-failed and partial-failed converter. The reconfiguration process introduces perturbations in the vector controlled AC drives. The paper tries to give a synthesis of the tandem vector control structure implementation. Problems related to hardware implementation of the transition from a control structure to another are discussed.***

## I. INTRODUCTION

In 1984 a new technology the Field-Programmable Gate Array (FPGA) for implementing digital logic was introduced. In the last years, they evolved from simple and inexpensive programmable logic devices (PLDs) to complex and reach-resource and sometimes-expensive devices. In the mean time, the applications, which first were mainly in implementing optimized two-level logic applications, today has developed to home networking, telecommunications, digital signal processing, and real-time control applications.

Many of the FPGAs were configured by static RAM cells, while other FPGAs were configured using antifuse technology. Antifuse-based FPGAs also were used for many applications because were much more attractive, thus smaller and faster due to less programming overhead, because there was no volatility to the configuration. Today the volatility has become a need in some applications and programming is no more considered a liability [2].

The new technology and the programming methods of the FPGA chips, which are named reconfiguration of the FPGA, and has generated a new research field named *reconfigurable computing*.

Accordingly to the definition the reconfigurable systems are those computing platforms whose architecture is modified by the software to suit the application at hand. This means that within the application program a software routine exists, that downloads a digital design directly into the reconfigurable space of the system [2, 4].

Traditionally, digital processing tasks were implemented in digital signal processors (DSP) using software implementation methods. Since the DSP is optimized for digital signal processing, however is not optimized for the specific algorithm, the algorithm implemented in software, may result in poor performance. While implementing the specific algorithm in hardware, is 'tailored' to the specific algorithm, resulting in fast performance. The invention of FPGA has given rise to an alternative method of computing. The FPGA provides the means for achieving hardware performance and software versatility. The FPGA implementation can be optimized for the specific algorithm, and can reuse and re-optimize multiple algorithms simply reconfiguring the device.

At the beginning of the 'FPGA era' most of reconfigurable computing systems were plug-in boards made for standard computers and they acted as a coprocessor attached to the main micro-processing unit.

Most of applications of reconfigurable computing were reported in image processing, digital signal processing and custom computing machines. With the evolution of FPGA technology and the associated design tools, the application field has grown rapidly. Even more, this technology became a support for the new single chip solution called System on Chip (SOC).

In the mid 1990s the evolution of FPGAs allowed the implementation of simple digital signal processing algorithms, and as a result of this possibility they have been introduced in motor control field.

First *Herbert* and *Beierke* announced the implementation of a universal PWM-unit (Pulse Width Modulation) [5]. The first application of FPGAs in motor control intended to implement parts of the digital control algorithm in order to improve the performances of a control system implemented using digital signal processors [1]. With the increase of the programmable logic device speed and capacity, it became possible the implementation in FPGA of a control system as a whole.

*Kiel* and *Lenze* observed the tendencies in control electronics for motor control systems and traced the future

trends [15]. They predicted the increasing importance of the FPGA chips in motor control implementations.

Up to now Cirstea, Imecs, Monmasson, Poure and their research groups reported application of reconfigurable hardware in the implementation of motor control system for AC Drives [3, 6, 17 and 18]. Considering that the main advantages of FPGAs regarding their reach-hardware resources and parallel algorithm implementation possibilities, but also in the run-time hardware-structure reconfiguration possibility, we may say it will be the basis of many future vector control applications. [16].

Reconfiguration of a control system may be necessary when a major failure occurs in the controlled plant or the changes in the control system variables demand much more effective control law and no adaptive control facilities are implemented [11, 23]. The need for reconfiguration is more evident if the controlled plant is of considerable importance (vital functions, high power, etc).

## II. RECONFIGURATION OF THE CONTROL SYSTEM

An alternative solution for medium- and high-power AC drives is the "tandem" static frequency converter (SFC) fed induction motor. This configuration is a hybrid SFC, which combines the advantages of two, parallel working, different types and different power ranges DC-link converters. A large power Current Source Inverter (CSI), operating in Pulse Amplitude Modulation (PAM) converts the active power, and a small power Voltage Source Inverter (VSI) working in Pulse Width Modulation (PWM) and supplies the reactive power required for improving the quality of the motor currents [12, 13].

To obtain the best dynamic behavior the control of the tandem-converter-fed induction motor can be achieved using conventional vector-control structures [12, 14].

Let suppose one of component converter (VSI or CSI) fails. This means, the control structure loses its tandem character and the control structure will work with only one inverter. Under these new working conditions, the control structure previously applied to the tandem converter is no more efficient. To keep the drive working the control structure need to be reconfigured corresponding to the working inverter character [22].

Due to the reconfiguration, the vector control system is implemented in Field Programmable Gate Array. Unlike other vector control system implementations [3, 17 and 18] the implementation presented in this paper exploits all the parallelism of the vector control algorithm. For this reason the hardware resources consumed by the implementation are very high. The advantage of parallel implementation is the high performance of the control system and the possibility to obtain very short sampling periods. The performance of the vector control system is limited only by the AD converter performances.

The reconfiguration of a vector control system can be motivated by the fail-safe operation of a plant. The plant (i.e. the control system, the inverter(s), the motor and the sensors) has to be kept on working in order to finish 'its mission'. In this case, *the reconfiguration moment $t_r$ is not known and the next configuration is known*. This reconfiguration case is applied to the tandem converter if one of the inverters (VSI or CSI) fails. This means, that the control structure loose its tandem character and the control structure will work with only one inverter. Under these new working conditions, the control structure previously applied to the tandem converter is no more valid. To keep the motor working the control structure need to be reconfigured corresponding to the working inverter character. As the tandem component inverters are the CSI and the VSI, result two new configuration states conform the reconfiguration state machine presented in *Fig. 1*. The figure presents the state transition graph for the tandem converter together with the reconfiguration conditions. Note that the main working control structure is the tandem converter (*STATE1*), and the need for reconfiguration is motivated with the failure of one of the inverters. For this reason, there is no reconfiguration from the *STATE2* to *STATE3* and vice versa (but theoretically we should consider these transitions also).

The power-on initialization i.e. starting the drive, it is realized, that either starting the control system with the tandem converter, or either starting it with CSI converter structure. This resulted from the obtained simulation results. Up to now the state transition graph was presented in [11, 13] with the power-on init in *STATE1*. New results proved that the start and power-on-init is imposed by the value of the starting currents, which can be very high and depends on the control structure. For this reason in some circumstances the start should be made with the CSI/VSI (*STATE2* or *STATE3*) inverter and after the system achieves its nominal working conditions it should be reconfigured for the tandem converter structure.

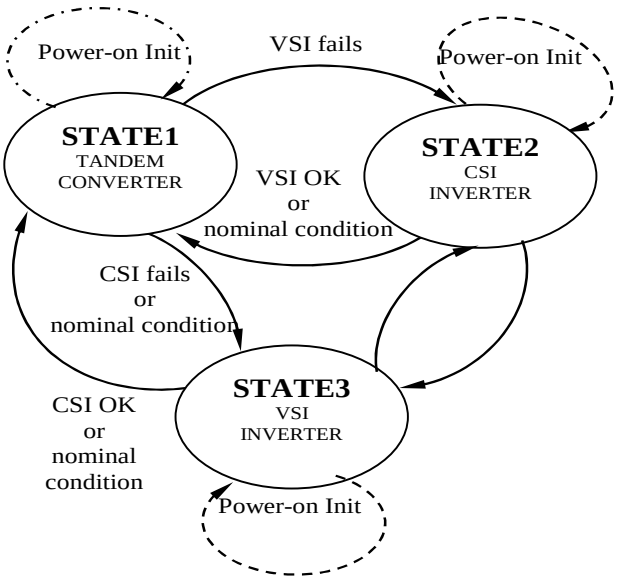


Fig. 1. The state transition graph of the tandem converter system

The tandem converter needs different control strategies depending on the type of the PWM procedure used for the VSI. The selected PWM procedure can change the source character of the VSI and of the tandem converter, too [9]. The open-loop voltage-control PWM procedures, i.e. carrier wave or Space-Vector Modulation (SVM), keep the voltage-source character of the VSI, but using closed-loop current-control PWM procedures (e.g. the common bang-bang current control) the behavior of the VSI becomes of current-source character.

The tandem converter is sensible to the VSI failure. If the VSI fails then the control system structure loose its voltage character and needs to be reconfigured in order to keep on motion the drive and to adapt the control system structure corresponding to the new demands. The CSI impose the new control structure character i.e. a current one.

The three fundamental criteria, determining the structure of a vector control system i.e. the orientation-flux, the field identification method, and the type of the used PWM procedure applied to command the converter, influence the control system structure of the tandem converter. For this reason, from the initially proposed tandem converter structure given by Trzynadlowski, Imecs et all. proposed different tandem structures. The transformation of these structures in reconfigurable ones resulted in completely new control system structures for AC drives [7, 10, 19 and 21]. The orientation flux (rotor - $\Psi_r$ or stator - $\Psi_s$) and the PWM method applied to the converter (i.e. space vector modulation or current feedback modulation) give three-reconfiguration possibilities as shown below in *TABLE I.*

There are two types of possible reconfiguration models - i.e. partial or total reconfiguration. The method is used in the implementations is a *total reconfiguration* for the CSoC and *partial reconfiguration* for the FPGA hardware support. For technological reasons, during the research process, simulation and implementation the *total reconfiguration* model was chosen, which reconfigures the control system as a whole.

TABLE I.
RECONFIGURATION POSSIBILITIES OF THE TANDEM CONVERTER

| ***CSI-fed motor*** | ***Tandem converter/VSI-fed motor*** | | ***Description*** |
|---|---|---|---|
| ***State 2*** | ***(State 1)*** | | ***in references*** |
| ***Orientation Flux*** | ***Orientation Flux*** | ***PWM Method*** | |
| Ψr | Ψr | SVM | [7,20] |
| Ψr | Ψs | SVM | [10, 19, 21] |
| Ψr | Ψr | Current Feedback Modulation ("bang-bang") | [8] |

The basic idea is straightforward: After power-up the control system of the AC drive works as 'tandem converter' (*STATE 1* of the state machine), when the VSI fails will be reconfigured to work as CSI converter (*STATE2* of the state machine). A possible representation of the transition from one state to the other, in fact, may be a demultiplexer and a multiplexer. However, one should note that, while these components may be indeed possible implementations, *they are intended to be abstract entities did not need any implementation*.

## III. CURRENT CONTROLLED PWM-VSI-FED INDUCTION MOTOR WITH ROTOR-FIELD ORIENTATION

Due to the voltage-source character of the tandem converter, the motor absorbs freely its stator currents. Consequently, the **VSI** will be the actuator ensuring the vector control of the induction motor drive. It is possible to apply the common PWM procedures (voltage- or current controlled ones) characteristic to the **VSI**.

Applying to the **VSI** current-controlled-PWM, in manner of the "bang-bang" converter, the tandem-converter-fed motor will be controlled in fact in current. Constant switching frequency is obtained using synchronized on-off switching controllers. The above-mentioned procedures are appropriate for field-orientation-based tandem-fed drives.

In *Fig. 2* the induction motor operates supplied from the both converters in tandem mode (corresponding to position 1 of the multiplexers). Supposing a failure of the **VSI** the control structure has to be adapted to the new working condition, i.e. running supplied only by the **CSI** (position 2 of the multiplexers). The reconfiguration of the hardware structure realizes the vector control system needed for the working inverters. Due to its simplicity, both operating modes use rotor-field orientation. In the tandem-fed mode, the **VSI** operates with current feedback loops.

Because of the difficulties encountered by direct measurement of the modulated-voltage waves, the stator voltage is identified in block $\boldsymbol{V_sId}$ using the measured DC-link voltage and the state of inverter switches according to the PWM logic taking into account the voltage losses on semiconductor devices, too.

Based on the stator-voltage and current components transformed in *d-q* reference frame, the block $\boldsymbol{\Psi_sC}$ integrates the natural stator-voltage equations yielding at its outputs the stator-flux *d-q* components. In order to obtain the orientation flux, the block $\boldsymbol{\Psi_rCo}$ compensates the stator flux.

The vector-analyzer $\boldsymbol{VA_2}$ computes the amplitude and the angular position of the orientation field.

The reference values of the stator-current space-phasor components are obtained from the flux- and speed-control loops. After the coordinate transformation, they will be transformed to the three-phase references of the hysteresis dead band current-controllers [7, 8].

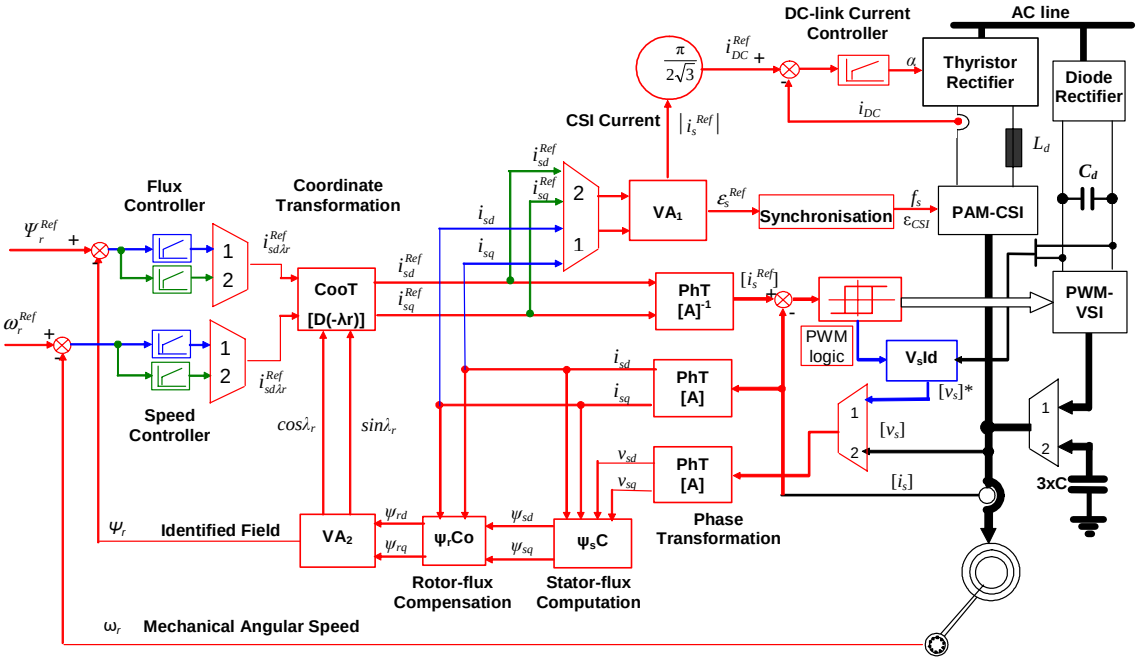


Fig. 2. Reconfigurable Rotor-field Oriented Vector Control System with Current Feedback Modulation for the Tandem Converter-Fed Induction Motor [8].

## IV. ALGORITHM ANALYSES AND MODULARITY

The creation of a module library was motivated by the fact that the simulation of the reconfiguration process is not possible or it is difficult while no tools exist for this kind of simulation. On the other hand, recently it has become possible to implement digital signal processing algorithms on FPGAs directly from Matlab Simulink® environment.

The elements of the library are the most common modules of vector control systems, and each present a standalone unit in the library. As a result of this independency, the vector control system can be synthesized by module or as a whole.

The modularity is important when the implementation target is reconfigurable hardware such as FPGAs [20]. Analyzing the work of parallel research groups *Cirstea* [3], *Monmasson* [18], *Pourre* [17] it can be concluded that those implementations were oriented for special purposes and they used configurable logic, but did not study the reconfiguration as a possibility for vector control systems.

The equations of vector control schemes can be decomposed in elementary mathematical operations. What is more, these elementary operations can be combined in the most used DSP function *"multiply and accumulate":*

$$c = \sum_{i=1}^{k} (a_i \times b_i) \qquad (1)$$

The difference between the DSP and FPGA implementation of the MAC is that in the case of latter one the operations from (1) are executed in parallel and not sequentially. In such a way, the execution time is reduced by the parallel computation.

Taking into account these circumstances, one can use two types of implementation topologies:

- sequential,
- parallel.

The parallel implementation of the algorithm results in very fast execution speed. For this reason, the sampling period can be decreased until the technology and the PID controllers allow it. The parallel computation of equations gives a significant improvement compared to the DSP sequential computation. The parallel implementation method disadvantages could be the intensive hardware resource consuming and the price paid for a chip. However, with the technology advances, the prices will decrease and the number of equivalent logic gates/chip will increase. Another advantage of the parallel implementation is that partial reconfiguration became possible for each computation module. This allows only the parts of the control system to be reconfigured, which are not common for two control structures. We can conclude that from the point of view of the reconfiguration, independent from which type of reconfiguration method is used, the parallel implementation is the optimum one.

The sequential implementation methods do not allow very short sampling periods comparing to the parallel one. The execution speed of the MAC functions has to be fast

enough, in order to compute all the equations of the control system in only one sampling period time. From the view point of reconfiguration the sequential implementation method is not an optimal solution. This is explained by the fact that the reconfigurations of the vector control system involve changes in the output variable characteristics (voltage/current) and modify the type and value of variables and constants when the new MAC functions are executed.

From the above reasoning results that the parallel implementation was chosen as a solution for the implementation of the IP library and the reconfigurable vector control system. Some functions of the vector control system cannot be implemented with the above-mentioned MAC function, in these cases particular solutions are applied. In *TABLE II* there are shown the implementation results of the module library and the estimated hardware resources needed for the implementation of the control system shown in *Fig. 2*.
In *TABLE II* there are presented the FPGA slices needed for the implementation of each module, the computation delay introduced by the modules, the quantization error and the maximum working frequency. One may say that the Vector analyzer modules are the most complex implementation from the point of view of the consumed resources (1995 slices). The fastest module is the PWM block. There are some modules were the implementation environment did not gave any information about the maximum working frequency and about the worth path delay. The data format used in the implementation was the Q16 fixed point data format (4.12).

The implementation of the vector control system given in *Fig. 2* is also shown in *TABLE II* and can be concluded that the total number of 4496 slices is not very high. With new FPGA families this control system can be implemented in a single chip. The maximum working frequency of the implemented tandem converter will be 38.45 MHz.

## V. SIMULATION RESULTS

In all the three possible reconfiguration variants presented in *TABLE I*, the simulations were performed with similar conditions in MATLAB-Simulink environment. The motor data are: 5.5 *kW*, 50 *Hz*, 220 *Vrms*, 14 *Arms* and 4 pole-pairs.

The motor was started controlled by the tandem inverter and after some time (usually 0.5s or 1s after start) the control structure was reconfigured due to the failed **VSI**. The simulations were concentrated on the moment of the reconfiguration and the effects on the motor variables if the control structure is reconfigured. The research was not extended to the fault detection, which is not the subject of this research. We presumed that the moment when the **VSI** fail could be detected in a way (for example detecting the equality of three voltages $u_{sa}=u_{sb}=u_{sc}=0$ at the same time).

The simulation results presented in this paper were made for the control scheme presented in *Fig. 2*. The simulation results show that the transients introduced by the reconfiguration influences all the variables as presented in [19].

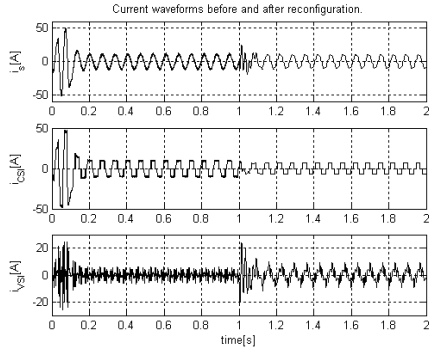


Fig. 3. Current waveforms before and after reconfiguration.

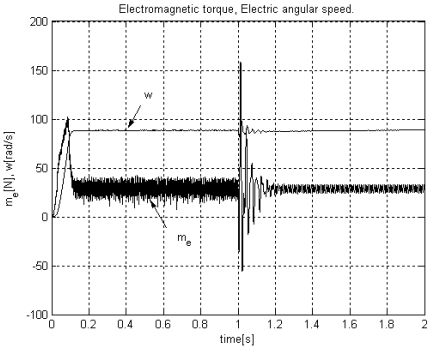


Fig. 5. Electromagnetic torque, Electric angular speed.

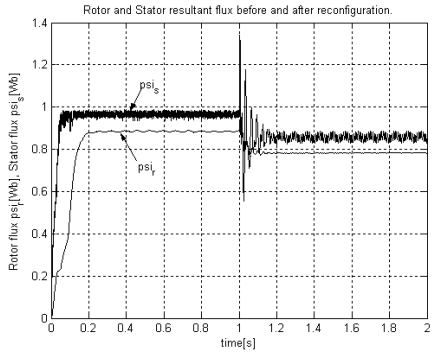


Fig. 4. Rotor and Stator resultant flux before and after reconfiguration.

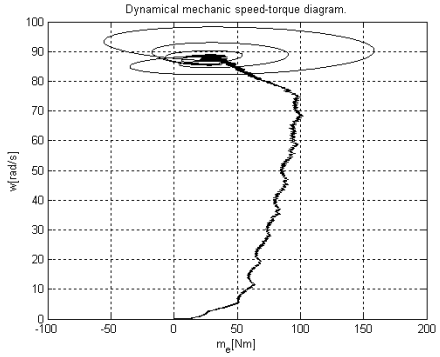


Fig. 6. Mechanical characteristics of the induction machine

TABLE II.
CHARACTERISTICS OF THE IMPLEMENTED VECTOR CONTROL LIBRARY MODULES.

| **Library element IP Module name** | **Symbol Name** | **Slices needed for implementation** | **Worth path delay introduced $t_d$[ns]** | **Quantization error** | **Max. working f[MHz]** |
|---|---|---|---|---|---|
| Direct Phase Transformation Block | PHT[A] | 152 | 27.00 | $q_e<1.5*10^{-4}$ | n.a |
| Reverse Phase Transformation Block | $PHT[A]^{-1}$ | 217 | 4.90 | 0 | n.a |
| Stator+Rotor-flux Compensation | $\Psi_s+\Psi_r Co$ | 1000 | 41.70 | $-0.02<q_e<0.1$ | 42,00 |
| Vector Analyzer | VA | 1995 | n.a. | n.a | 166,90 |
| Coordinate Transformation | $CooT[D(\pm\lambda_r)]$ | 25 | 10.00 | $<1.\ 10^{-4}$ | n.a |
| Space Vector Modulation | SVM | 27 | 3.06 | ~0 | n.a |
| Current feedback Modulation | PWM | 77 | 31.20 | | 224.15 |
| Flux Controller | Ψ-PI | 24 | 4.00 | $\sim 0.6*10^{-4}$ | n.a |
| Speed Controller | Ω-PI | 24 | 4.00 | $\sim 0.6*10^{-4}$ | n.a |
| Flux+Speed Controller | PI | 135 | 13.73 | $q_{eflux} \cong -6*10^{-3}$ $-0.1<q_{espeed}<0.16$ | 128.18 |
| DC-link Current Controller | DC-PI | 298 | 24.00 | | 86.70 |
| Reconfiguration Multiplexer | MUXr | 5 | 3.12 | 0 | n.a |
| CSI current constant multiplier | K1 | 79 | 16.99 | $-2*10^{-5}<q_e<5*10^{-5}$ | n.a |
| Estimated implementation resources for *Fig. 2* | Tandem | 4496 slices 1058 FF 9334 LUT | - | - | 38.45 |

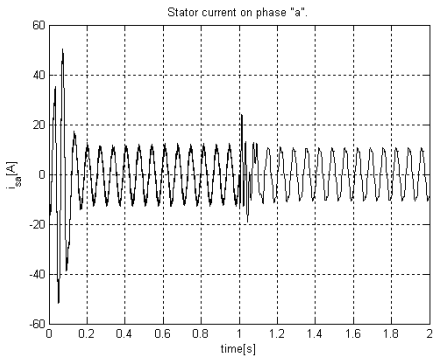


Fig. 7. Stator current on phase "a".

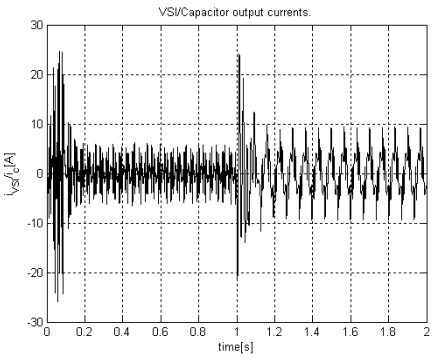


Fig. 8. VSI/Capacitor output currents.

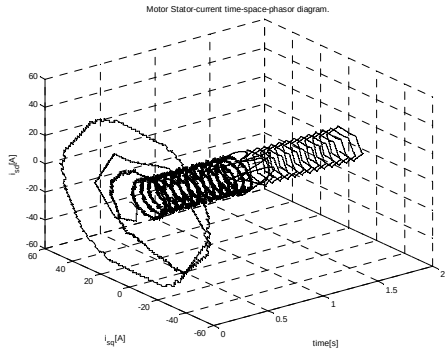


Fig. 9. Motor Stator-current space-phasor diagrams.

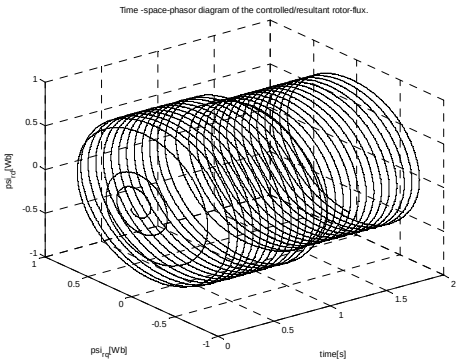


Fig. 12. Space-phasor diagrams of the controlled/resultant rotor-flux.

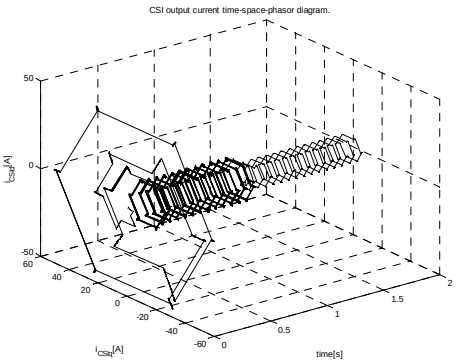


Fig. 10. CSI output current space-phasor diagrams.

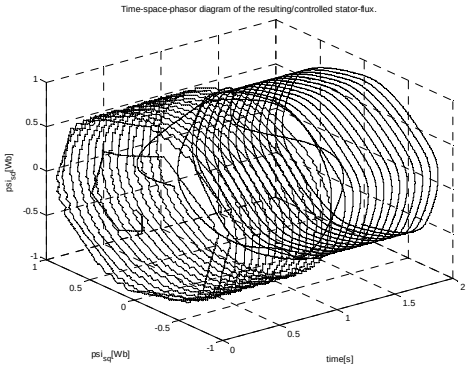


Fig. 13. Space-phasor diagrams of the resulting/controlled stator-flux.

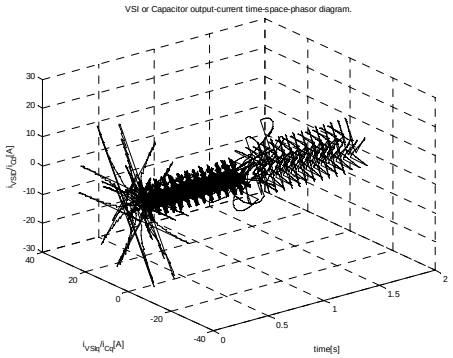


Fig. 11. VSI or Capacitor output-current space-phasor diagrams.

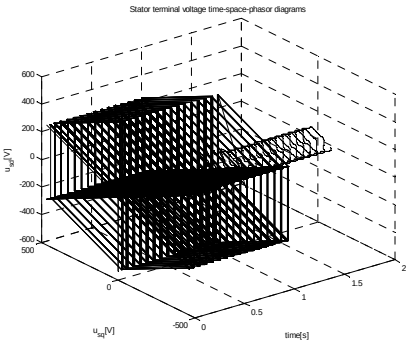


Fig. 14. Stator terminal voltage space-phasor diagrams.

From the simulation results one can conclude that the transition from one control structure to the other generate transients in the motor. A transient management solution was proposed in [21]

## VI. CONCLUSIONS

The reconfigurable vector control system for tandem inverter is a new solution for AC drives. It improves the working conditions of the drive, also assures fail safe operation.

Vector control systems for AC drives are characterized by high dynamic performance. For the reconfiguration of such a system yet it is technologically impossible to compile the next configuration in run-time. The reconfiguration is applicable only if the next configuration is known at compile time, while the duration of the actual configuration is unknown or can not be predicted.

Since the simulation of the reconfiguration process in MATLAB® Simulink environment was modeled by multiplexers. In the implementation these multiplexers were implemented. In such a way a reconfigurable control algorithm was proposed.

The research concentrated on the fail of the VSI. If the CSI fail the vector control system together with the VSI and the motor still can work, but the performances will be lower then the tandem inverter performances.

For implementation of reconfigurable vector control structures CSOC and FPGA chips are recommended. The created Module Library, like other Matlab® tools, helps the rapid prototyping and implementation of vector control systems for AC drives targeting FPGA chips. The module parameters are freely modifiable on demand.

The Module Library allows the simulation of the reconfiguration process and the study of the reconfiguration effects upon the behavior of the AC drives.

Comparing with other existing FPGA implementations the implementation results presented in this paper allows the parallel implementation of any vector control system, in contrast with other implementations based on sequential computation. Similar results using parallel implementation were presented in [25, 26]. The advantage of parallel implementation is the increased computation speed and low sampling period. The disadvantage may be considered the high number of FPGA cell consumption, which implies the use of rich resource FPGA chips.

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