Boolean

Variant: Prototype

10/22/2020

V2I1

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

Title: Boolean		***Variant:*** Prototype	
Page Contents: [01] - COVER PAGE.SchDoc			
Size: A4	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
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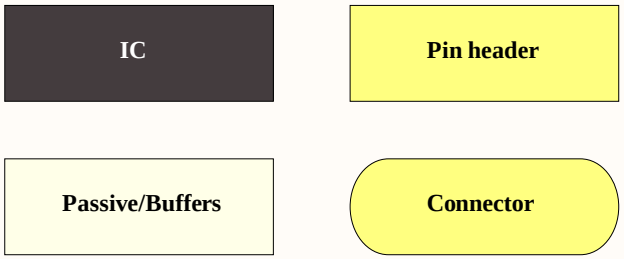
Boolean
(Block Diagram)

Legend



Title: Boolean		***Variant:*** Prototype	
Page Contents: [02] - BLOCK DIAGRAM.SchDoc			
Size: A4	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
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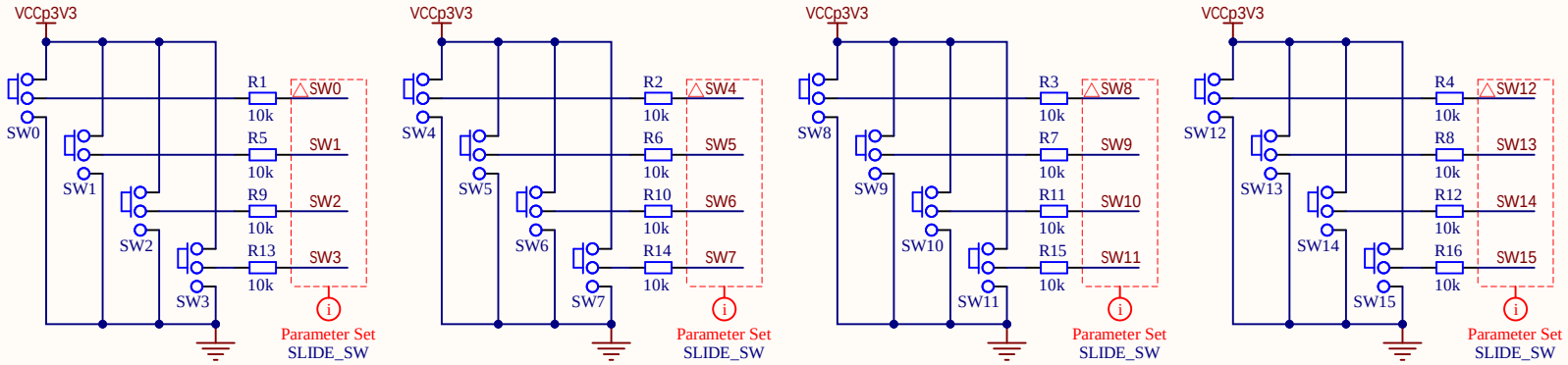
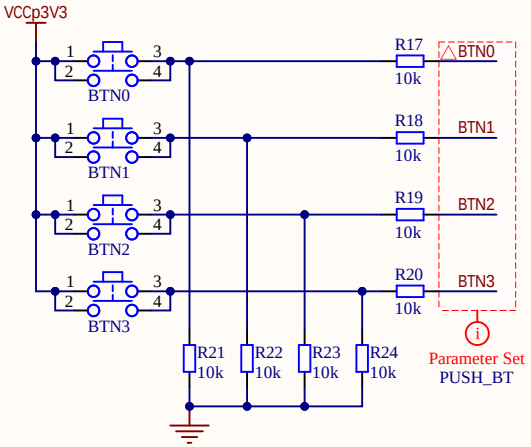
SWITCHES, BUTTONS





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Title: Boolean		***Variant:*** Prototype	
Page Contents: [03] - BTNs, SWs.SchDoc			
Size: A4	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
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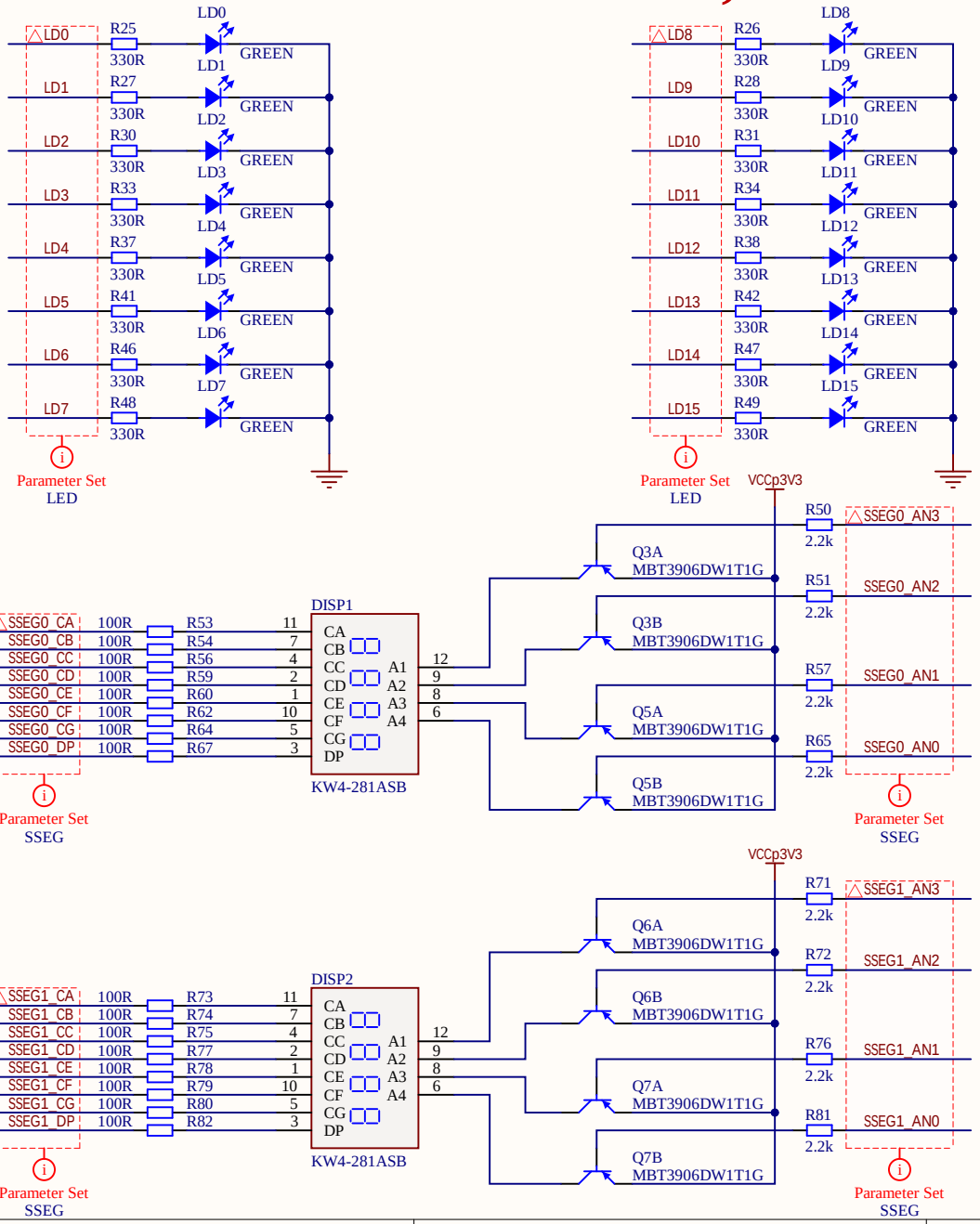
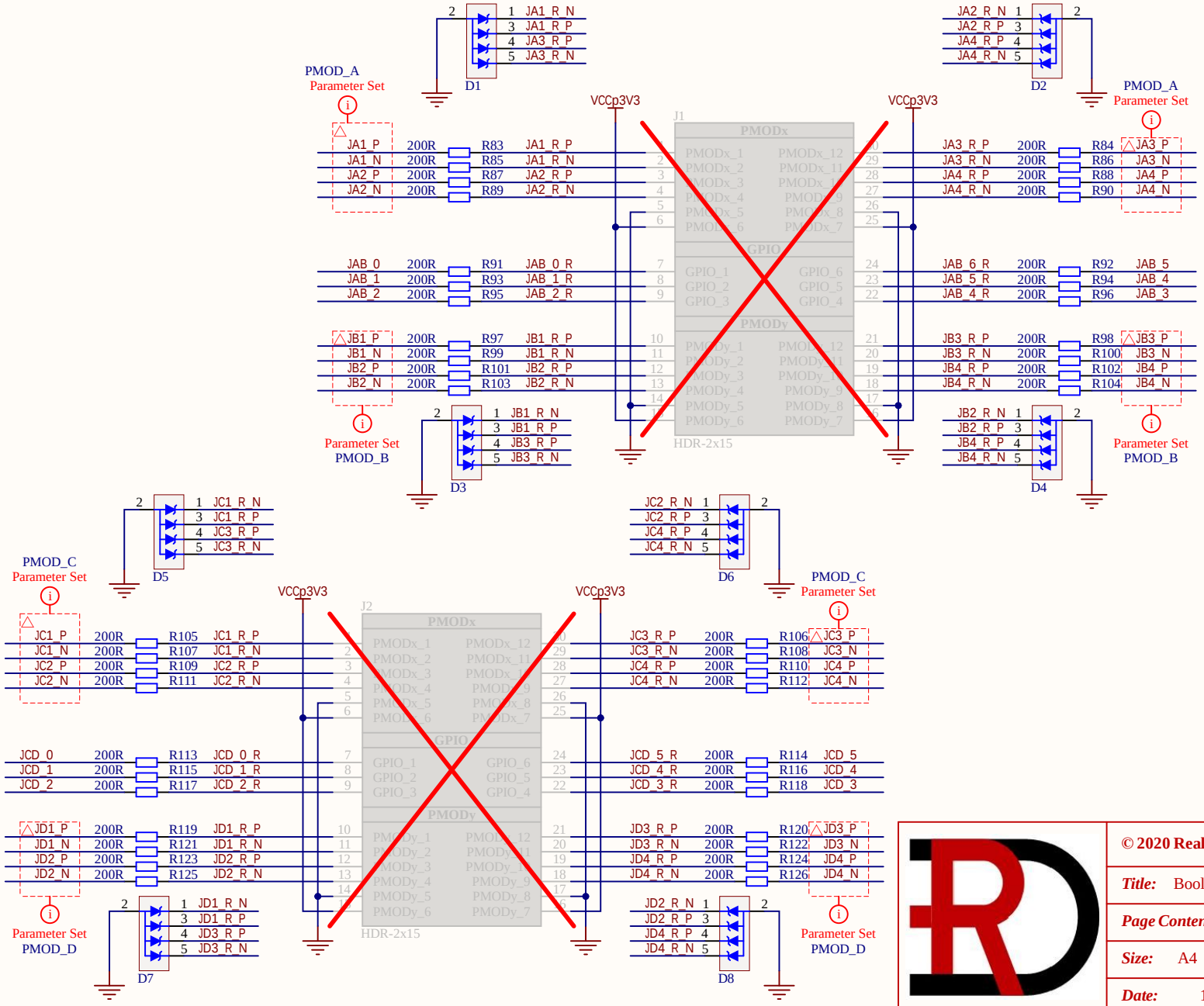
LEDs, SEVEN-SEGMENT



Title: Boolean		***Variant:*** Prototype	
Page Contents: [04] - LEDs, SSEG.SchDoc			
Size: A4	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 10/22/2020	***Checked by:*** *	***Sheet*** 4 ***of*** 17	

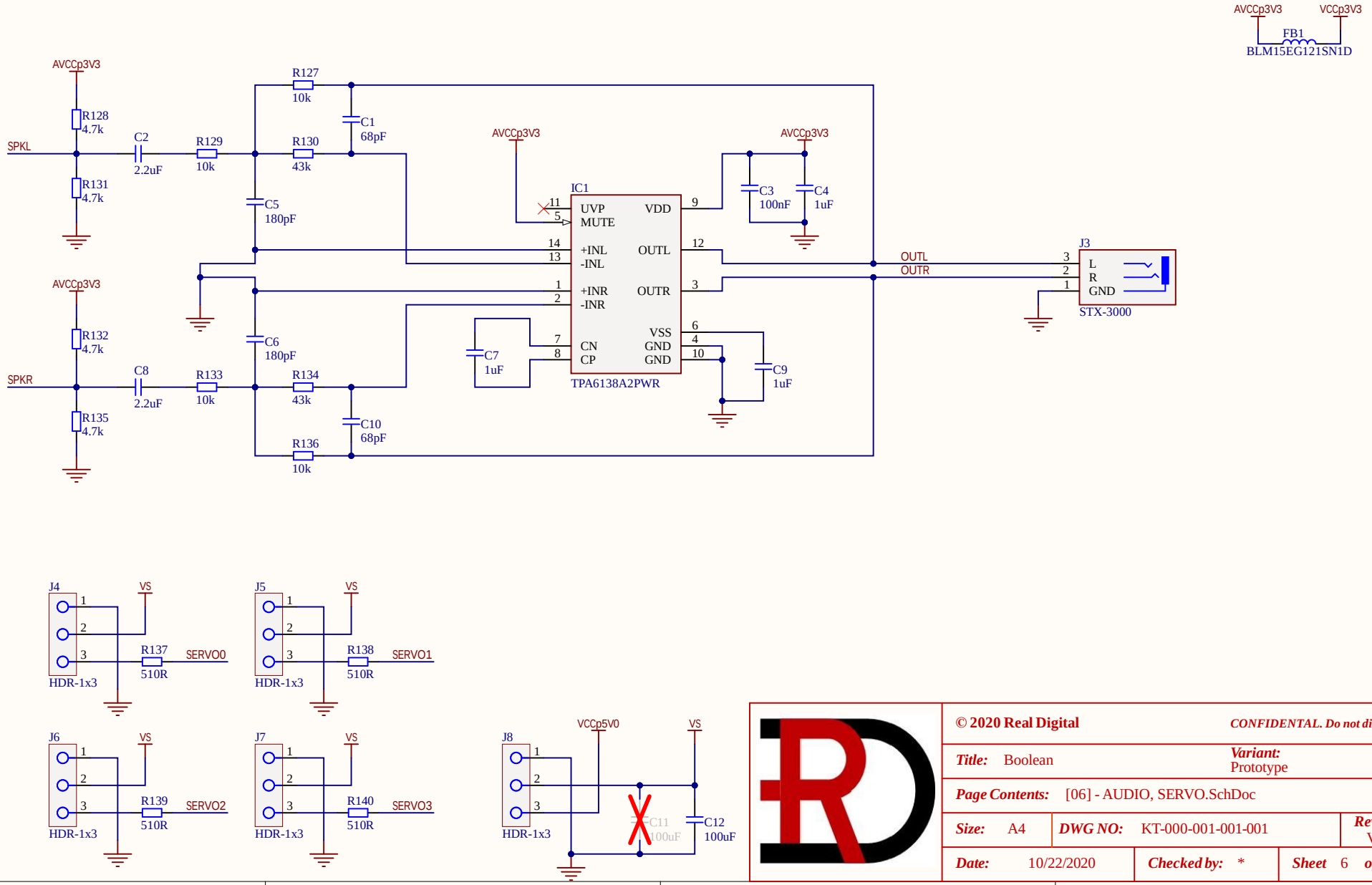
PMODs



CONFIDENTAL. Do not distribute.

Title: Boolean		***Variant:*** Prototype	
Page Contents: [05] - PMOD.SchDoc			
Size: A4	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 10/22/2020	***Checked by:*** *	***Sheet*** 5 ***of*** 17	

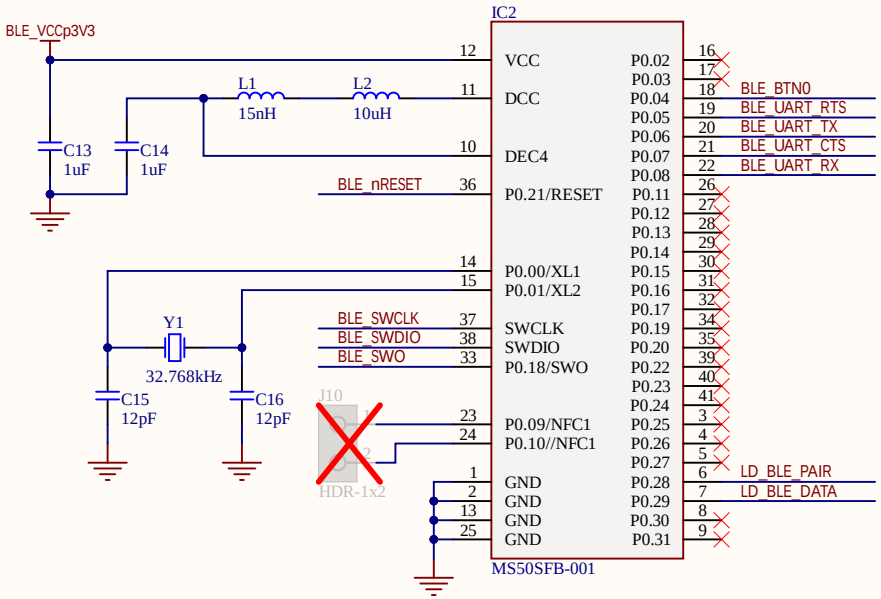
AUDIO, SERVO

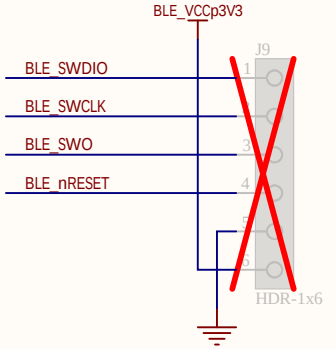


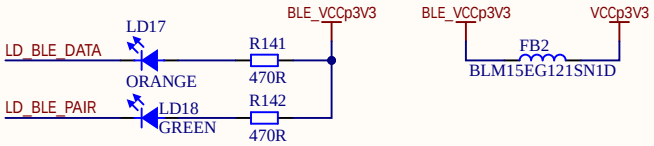
CONFIDENTAL. Do not distribute.

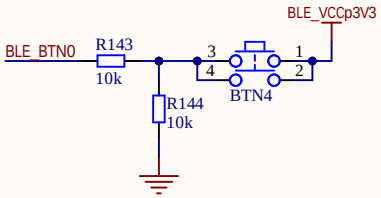
Title: Boolean		***Variant:*** Prototype	
Page Contents: [06] - AUDIO, SERVO.SchDoc			
Size: A4	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 10/22/2020	***Checked by:*** *	***Sheet*** 6 ***of*** 17	

BLE MODULE



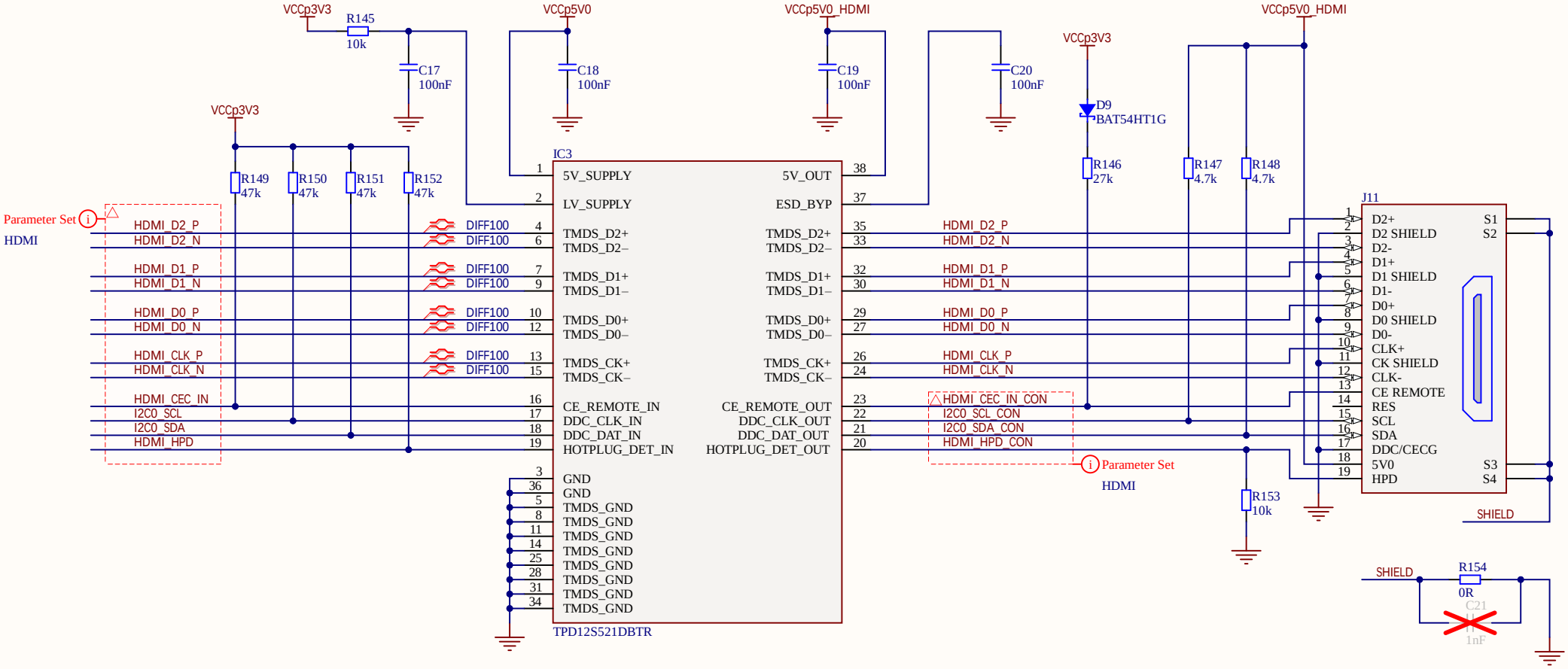






Title: Boolean		**Variant:** Prototype
Page Contents: [07] - BLE MODULE.SchDoc		
Size: A4	**DWG NO:** KT-000-001-001-001	**Revison:** V2I1
Date: 10/22/2020	**Checked by:** *	**Sheet** 7 **of** 17

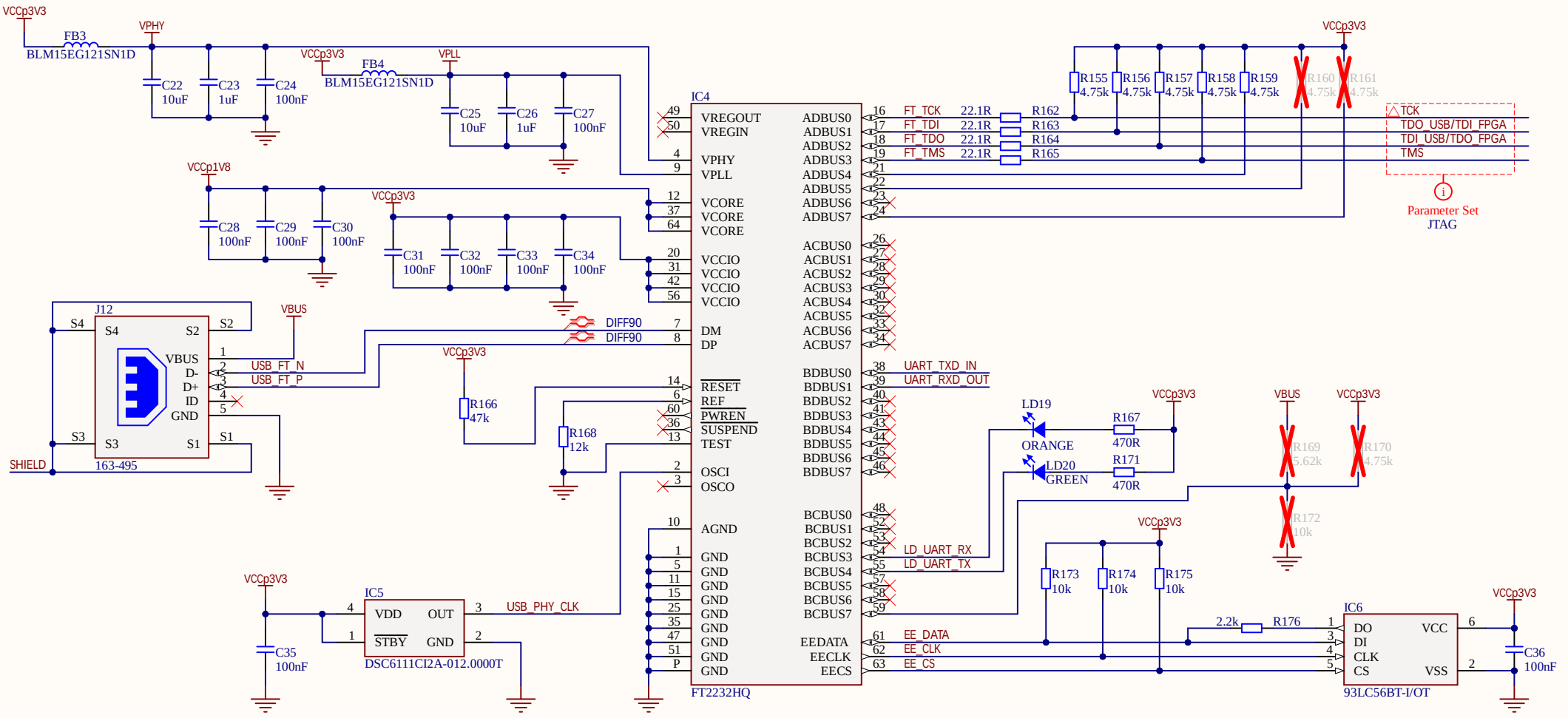
HDMI



CONFIDENTAL. Do not distribute.

Title: Boolean		***Variant:*** Prototype	
Page Contents: [08] - HDMI.SchDoc			
Size: A4	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 10/22/2020	***Checked by:*** *	***Sheet*** 8 ***of*** 17	

USB-JTAG, USB-UART



Title: Boolean		**Variant:** Prototype
Page Contents: [09] - USB-JTAG, USB-UART.SchDoc		
Size: A4	**DWG NO:** KT-000-001-001-001	**Revison:** V2I1
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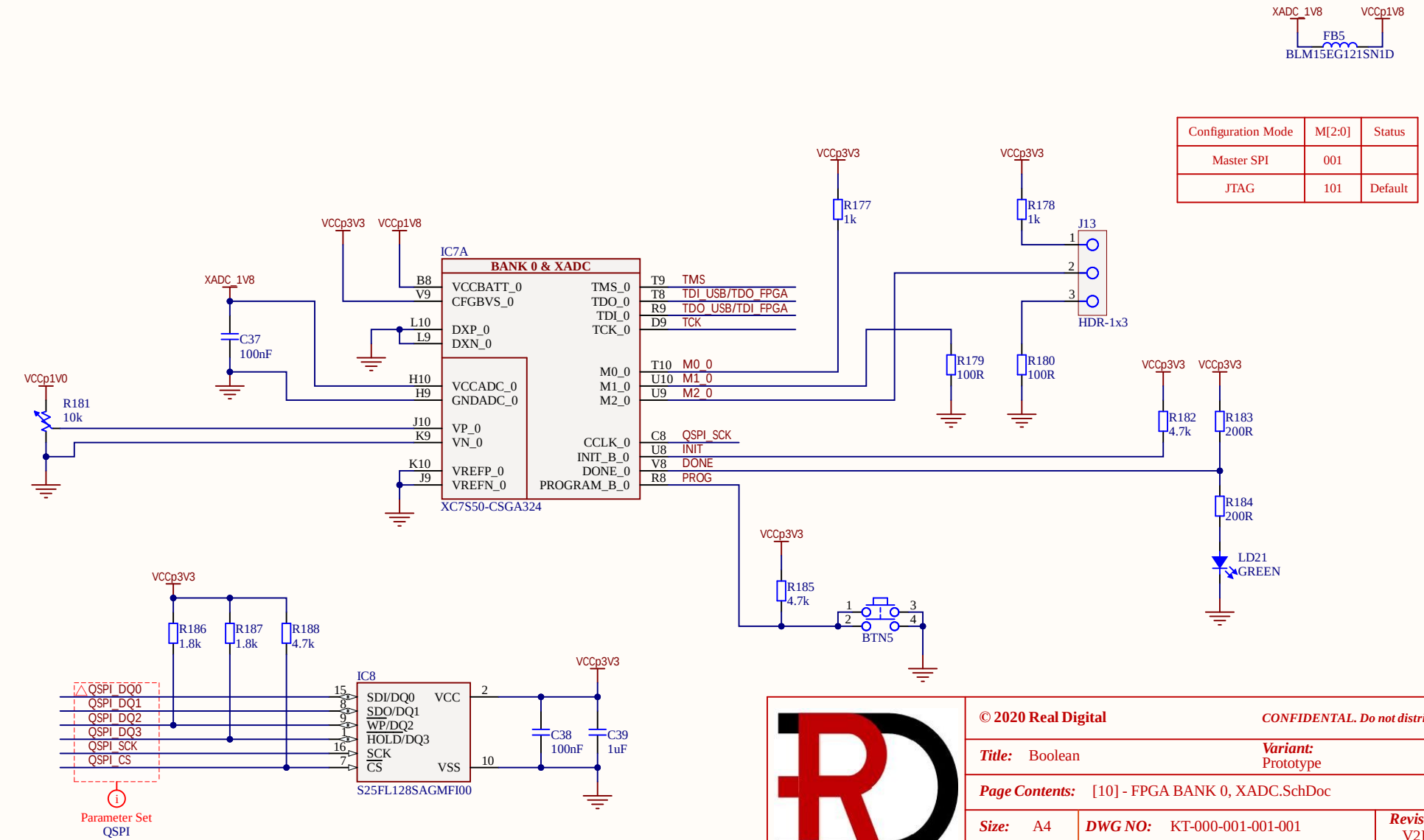
FPGA BANK 0 , XADC



Title: Boolean		**Variant:** Prototype
Page Contents: [10] - FPGA BANK 0, XADC.SchDoc		
Size: A4	**DWG NO:** KT-000-001-001-001	**Revison:** V2I1
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FPGA BANK 14, 15 and 16

IC7B

BANK 14

IO_0_14	L13	
IO_L1P_T0_D00_MOSI_14	K17	QSPI_DQ0
IO_L1N_T0_D01_DIN_14	K18	QSPI_DQ1
IO_L2P_T0_D02_14	L14	QSPI_DQ2
IO_L2N_T0_D03_14	M15	QSPI_DQ3
IO_L3P_T0_DQS_PUDC_B_14	L15	SERVO2
IO_L3N_T0_DQS_EMCCLK_14	L16	SERVO3
IO_L4P_T0_D04_14	L17	
IO_L4N_T0_D05_14	L18	
IO_L5P_T0_D06_14	M14	SERVO0
IO_L5N_T0_D07_14	N14	SPKR
IO_L6P_T0_FCS_B_14	M13	QSPI_CS
IO_L6N_T0_D08_VREF_14	N13	SPKL
IO_L7P_T1_D09_14	M16	SERVO1
IO_L7N_T1_D10_14	M17	
IO_L8P_T1_D11_14	M18	
IO_L8N_T1_D12_14	N18	
IO_L9P_T1_DQS_14	P17	
IO_L9N_T1_DQS_D13_14	P18	
IO_L10P_T1_D14_14	R18	
IO_L10N_T1_D15_14	T18	
IO_L11P_T1_SRCC_14	P14	
IO_L11N_T1_SRCC_14	P15	
IO_L12P_T1_MRCC_14	N15	HDMI_D2_P
IO_L12N_T1_MRCC_14	P16	HDMI_D2_N
IO_L13P_T2_MRCC_14	R14	HDMI_CLK_P
IO_L13N_T2_MRCC_14	T14	HDMI_CLK_N
IO_L14P_T2_SRCC_14	R16	HDMI_D1_P
IO_L14N_T2_SRCC_14	R17	HDMI_D1_N
IO_L15P_T2_DQS_RDWR_B_14	U17	
IO_L15N_T2_DQS_DOUT_CSO_B_14	U18	
IO_L16P_T2_CSI_B_14	U16	
IO_L16N_T2_D31_14	V17	
IO_L17P_T2_D30_14	R15	HDMI_D0_P
IO_L17N_T2_D29_14	T15	HDMI_D0_N
IO_L18P_T2_D28_14	U15	
IO_L18N_T2_D27_14	V16	
IO_L19P_T3_D26_14	P13	
IO_L19N_T3_D25_VREF_14	R13	
IO_L20P_T3_D24_14	V14	
IO_L20N_T3_D23_14	V15	
IO_L21P_T3_DQS_14	U12	
IO_L21N_T3_DQS_D22_14	V13	
IO_L22P_T3_D21_14	T12	I2C0_SDA
IO_L22N_T3_D20_14	T13	I2C0_SCL
IO_L23P_T3_D19_14	R11	HDMI_CEC_IN
IO_L23N_T3_D18_14	T11	HDMI_HPD
IO_L24P_T3_D17_14	U11	UART_RXD_OUT
IO_L24N_T3_D16_14	V12	UART_TXD_IN
IO_25_14	R12	

XC7S50-CSGA324

IC7C

BANK 15

IO_0_15	G13	
IO_L1P_T0_AD0P_15	B13	JA1_P
IO_L1N_T0_AD0N_15	A13	JA1_N
IO_L2P_T0_AD8P_15	B14	JA2_P
IO_L2N_T0_AD8N_15	A14	JA2_N
IO_L3P_T0_DQS_AD1P_15	B15	JB1_P
IO_L3N_T0_DQS_AD1N_15	A15	JB1_N
IO_L4P_T0_15	B16	JB3_P
IO_L4N_T0_15	A16	JB3_N
IO_L5P_T0_AD9P_15	F12	JA3_P
IO_L5N_T0_AD9N_15	D12	JA3_N
IO_L6P_T0_15	C13	JA4_P
IO_L6N_T0_VREF_15	C14	JA4_N
IO_L7P_T1_AD2P_15	B17	JB2_P
IO_L7N_T1_AD2N_15	A17	JB2_N
IO_L8P_T1_AD10P_15	C17	JB4_P
IO_L8N_T1_AD10N_15	B18	JB4_N
IO_L9P_T1_DQS_AD3P_15	D16	
IO_L9N_T1_DQS_AD3N_15	D17	
IO_L10P_T1_AD11P_15	E16	
IO_L10N_T1_AD11N_15	E17	
IO_L11P_T1_SRCC_15	D18	JAB_5
IO_L11N_T1_SRCC_15	C18	JAB_0
IO_L12P_T1_MRCC_15	D14	
IO_L12N_T1_MRCC_15	D15	
IO_L13P_T2_MRCC_15	F14	UCLK
IO_L13N_T2_MRCC_15	F15	
IO_L14P_T2_SRCC_15	G16	
IO_L14N_T2_SRCC_15	G17	
IO_L15P_T2_DQS_15	E14	
IO_L15N_T2_DQS_15	E15	
IO_L16P_T2_15	F18	JAB_4
IO_L16N_T2_15	E18	JAB_1
IO_L17P_T2_15	F13	
IO_L17N_T2_15	E13	
IO_L18P_T2_15	H15	
IO_L18N_T2_15	G15	
IO_L19P_T3_15	K16	
IO_L19N_T3_VREF_15	J16	
IO_L20P_T3_15	H13	
IO_L20N_T3_15	H14	
IO_L21P_T3_DQS_15	H18	JAB_3
IO_L21N_T3_DQS_15	G18	JAB_2
IO_L22P_T3_15	H16	
IO_L22N_T3_15	H17	
IO_L23P_T3_15	K14	
IO_L23N_T3_15	J15	
IO_L24P_T3_RS1_15	J13	
IO_L24N_T3_RS0_15	J14	
IO_25_15	K13	

XC7S50-CSGA324

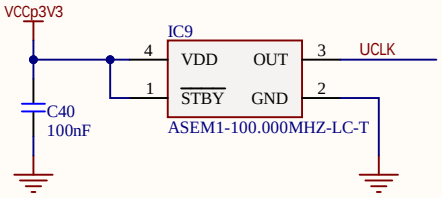
IC7D

BANK 16

IO_L6N_T0_VREF_16	D11
IO_L11P_T1_SRCC_16	C10
IO_L11N_T1_SRCC_16	C9
IO_L12P_T1_MRCC_16	A10
IO_L12N_T1_MRCC_16	A9
IO_L13P_T2_MRCC_16	C12
IO_L13N_T2_MRCC_16	C11
IO_L14P_T2_SRCC_16	B11
IO_L14N_T2_SRCC_16	A11
IO_L19N_T3_VREF_16	D10

XC7S50-CSGA324

DESIGN NOTE:
UG483: "For maximum ESD protection in an unused bank, all VCCO and I/O pins in that bank should be connected together to the same potential, whether that be ground, a valid VCCO voltage, or a floating plane."



Title: Boolean		**Variant:** Prototype	
Page Contents: [11] - FPGA BANKS 14, 15 and 16.SchDoc			
Size: A4	**DWG NO:** KT-000-001-001-001		**Revison:** V2I1
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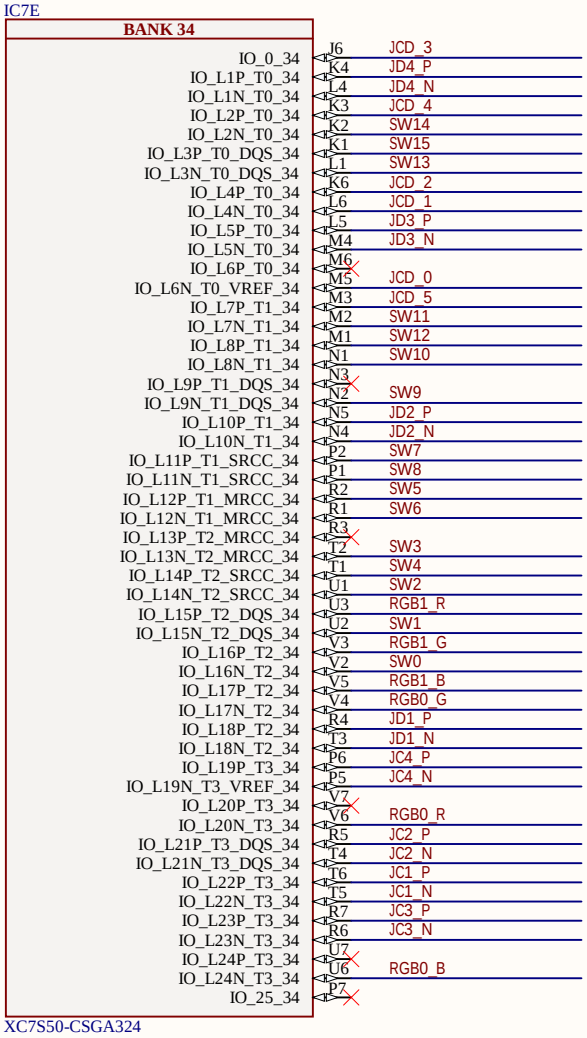
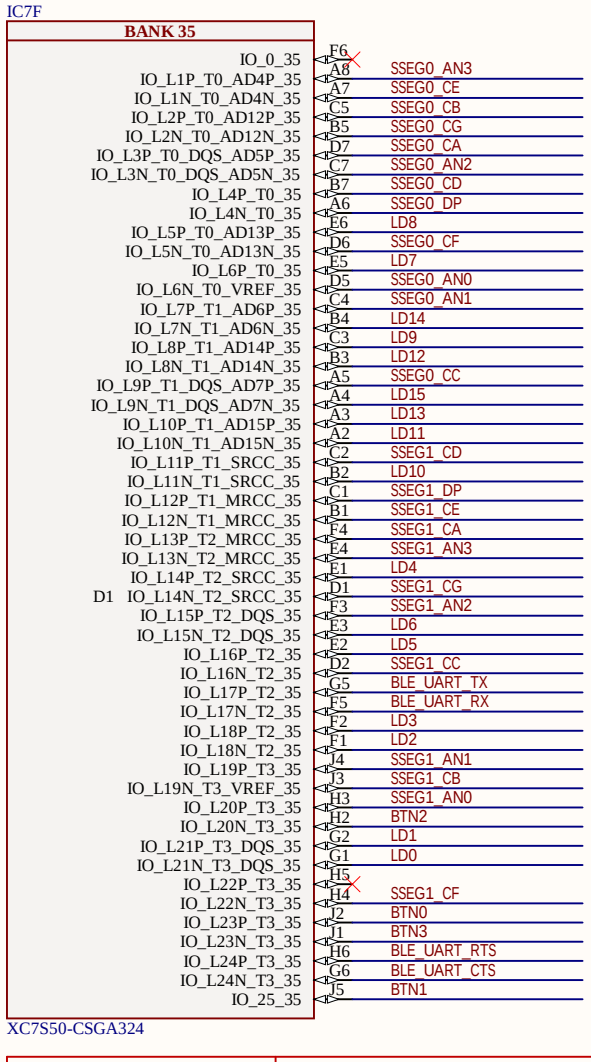
FPGA BANK 34 and 35





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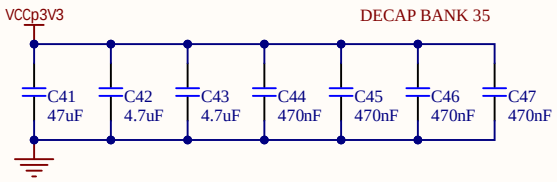
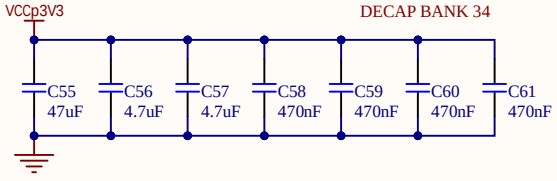
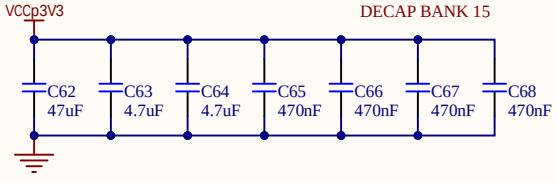
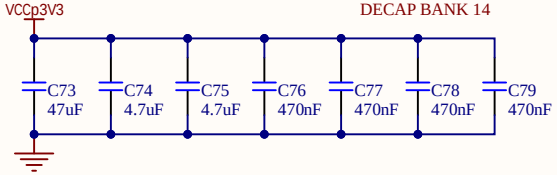
Page Contents: [12] - FPGA BANKS 34 and 35.SchDoc			
Size: A4	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 10/22/2020	***Checked by:*** *	***Sheet*** 12 ***of*** 17	

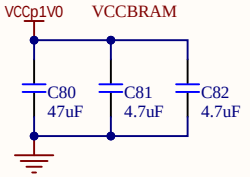
FPGA POWER

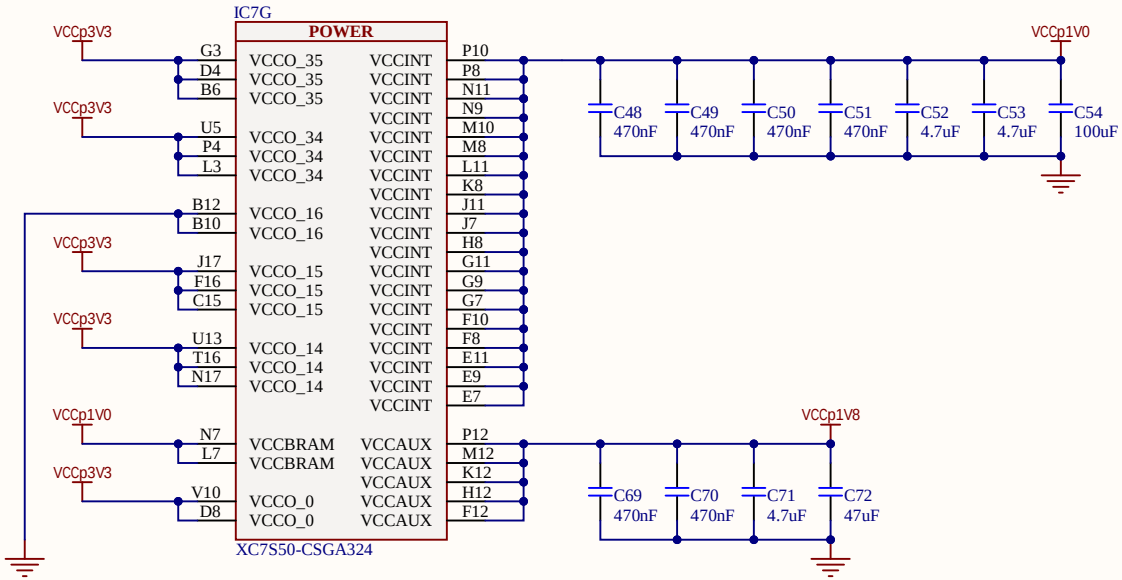


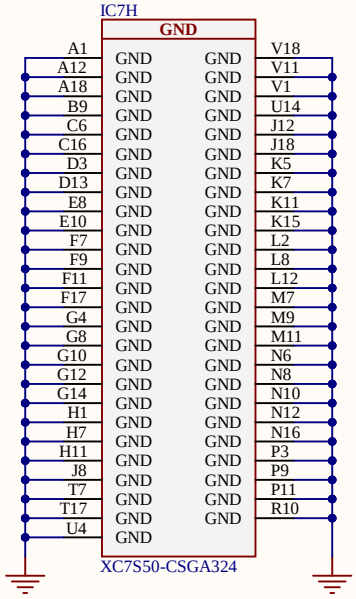






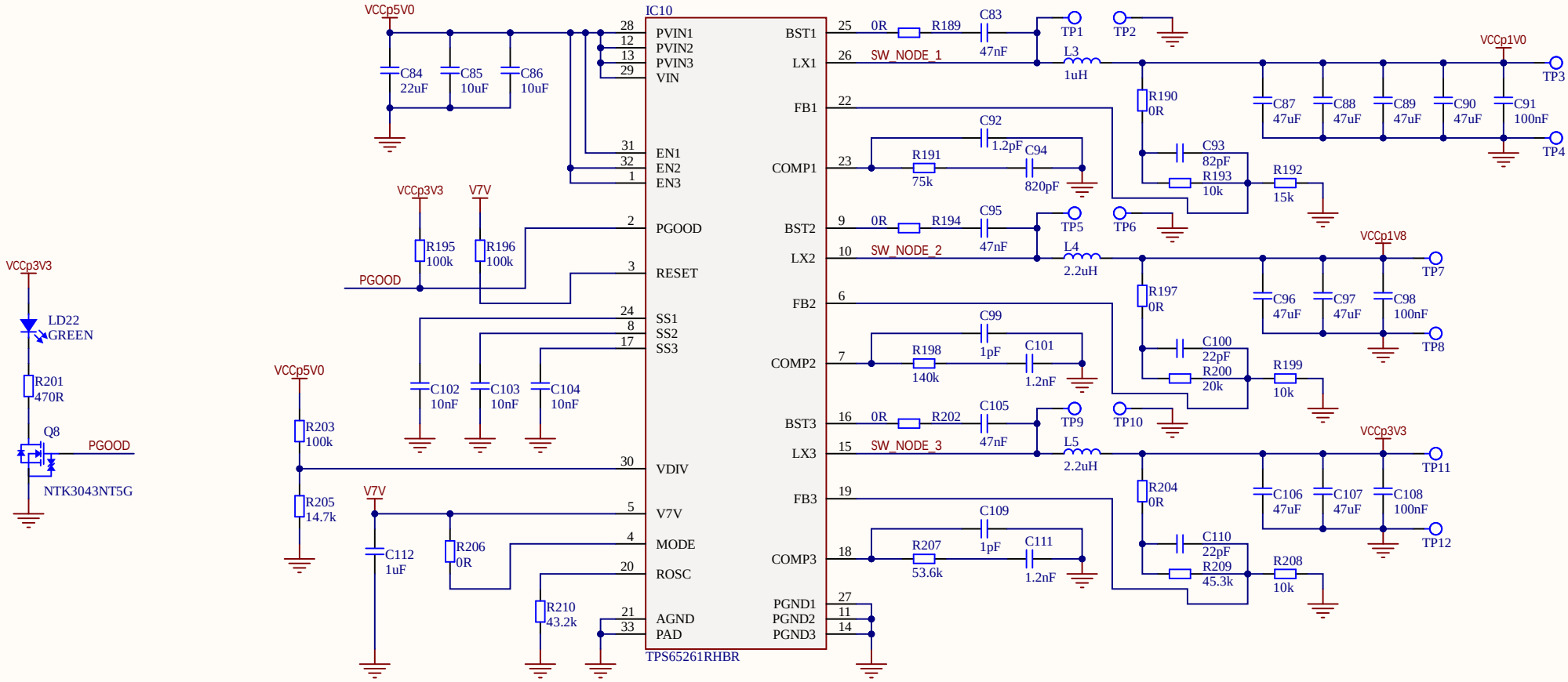






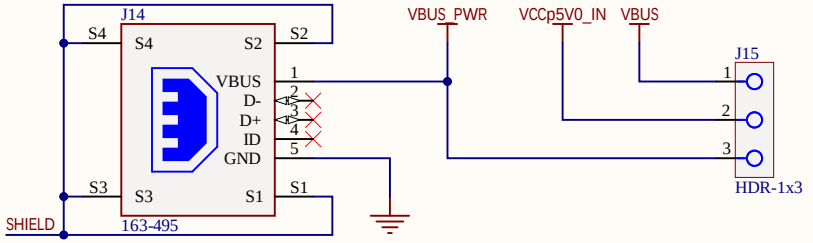
Title: Boolean		**Variant:** Prototype	
Page Contents: [13] - FPGA POWER.SchDoc			
Size: A4	**DWG NO:** KT-000-001-001-001		**Revison:** V2I1
Date: 10/22/2020	**Checked by:** *	**Sheet** 13 **of** 17	

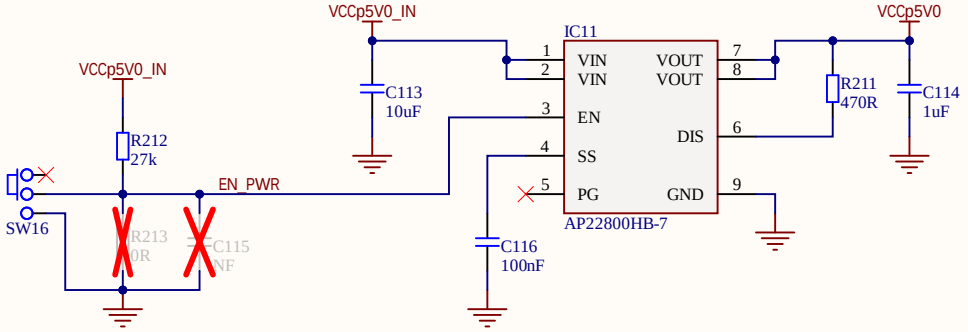
POWER I



Title: Boolean		**Variant:** Prototype	
Page Contents: [14] - POWER I.SchDoc			
Size: A4	**DWG NO:** KT-000-001-001-001		**Revison:** V2I1
Date: 10/22/2020	**Checked by:** *		**Sheet** 14 **of** 17

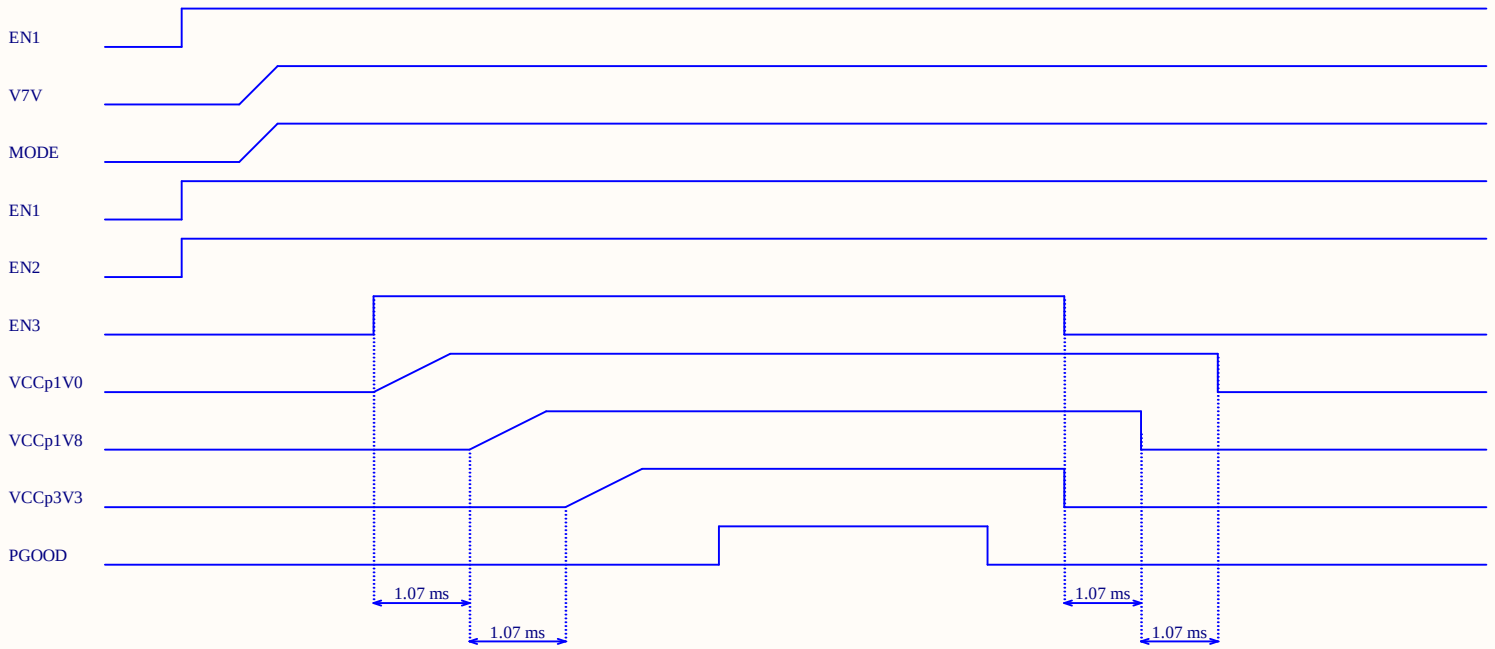
POWER II

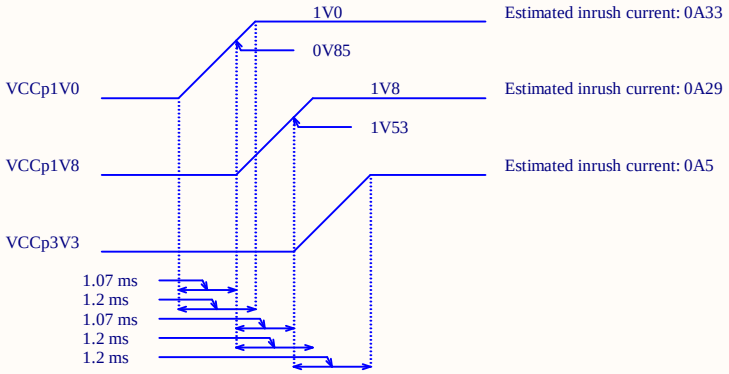




Title: Boolean		**Variant:** Prototype	
Page Contents: [15] - POWER II.SchDoc			
Size: A4	**DWG NO:** KT-000-001-001-001		**Revison:** V2I1
Date: 10/22/2020	**Checked by:** *	**Sheet** 15 **of** 17	

POWER SEQUENCING





QR Code Boolean QR1	Real Digital LG1	Rubber Feet STD1	Rubber Feet STD2
Boolean LG3	Xilinx LG2	Rubber Feet STD3	Rubber Feet STD4

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Title: Boolean		***Variant:*** Prototype
Page Contents: [16] - POWER SEQUENCING.SchDoc		
Size: A4	***DWG NO:*** KT-000-001-001-001	***Revison:*** V2I1
Date: 10/22/2020	***Checked by:*** *	***Sheet*** 16 ***of*** 17

DOC: REVISION HISTORY

CLOCKS (CPU & PCIE)

Title: Boolean		***Variant:*** Prototype	
Page Contents: [17] - DOC REVISION HISTORY.SchDoc			
Size: A4	***DWG NO:*** KT-000-001-001-001		***Revison:*** V2I1
Date: 10/22/2020	***Checked by:*** *	***Sheet*** 17 ***of*** 17	