4.6. Discrete cosine transform

DERIVATION OF THE 2-D DCT ALGORITHM

Definition of the 2-D transformation

$$[X] = [C]\ [x]\ [C]^T$$

[x], [X] are 2-D data structures, [C] is the transform matrix

$$C(m,k) = \sqrt{\frac{2}{N}}\, c(k) \cos\frac{(2m+1)k\pi}{2N} \qquad m,k, = 0,1,..N-1 \qquad c(k) = \begin{cases} \sqrt{2} & k \\ 1 & k \end{cases}$$

Typical 2 step algorithm for the 2-D DCT: N 1-D DCT -> Transposition -> N 1-D DCT

Direct 2-D algorithm in normal and matrix form

$$X(u,v) = \frac{2}{N} c(u)\, c(v) \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} x(i,j) \cos\frac{(2i+1)u\pi}{2N} \cos\frac{(2j+1)v\pi}{2N}$$

$$u,v,i,j = 0,1,\ldots,N-1; \qquad c(u), c(v) = \begin{cases} \sqrt{(2)} & u,v = 0 \\ 1 & u,v \neq 0 \end{cases}$$

$$X_L = [F]\, x_L \qquad [F] = [C] \otimes [C]$$

$$F(m,n) = \frac{2}{N} c(Q(m,N)) c(R(m,N)) \cos\frac{(2Q(n,N)+1)Q(m,N)\pi}{2N} \cos\frac{(2R(n,N)+1)R(m,N)\pi}{2N}$$

n,m=0,1,..N^2-1, Q(n,N), Q(m,N), R(n,N), R(m,N) quotients and remainder of the integer division, X_L and x_L are of N^2 size linear vectors of row by row scanned 2-D data structures

Basic steps of the derivation of the algorithm

$$\cos a \cdot \cos b = \frac{1}{2} \{ \cos(a+b) + \cos(a-b) \}$$

The [F] transformation matrix is separable

$$X_L = [F]x_L = ([F^+] + [F^-])x_L = [F^+]x_L + [F^-]x_L$$

Elements of [F+] and [F-] cover the same set of values

$$Ci = \cos\frac{i\pi}{2N}, \qquad i = 0,1,\ldots N-1$$

These separation can be continued until all the matrices contains only one Ci constant

$$X_L = ([F0^+] + [F1^+] + \ldots + [F(N-1)^+])x_L + ([F0^-] + [F1^-] + \ldots + [F(N-1)^-])x_L$$

From the generation method of [Fi$^+$] and [Fi$^-$] follows, that

$$Fi^{+}(m,n) \cdot Fi^{-}(m,n) = 0 \qquad i = 0,1,...N-1$$

so the appropriate matrices can be merged and the Ci values removed from Fi matrices

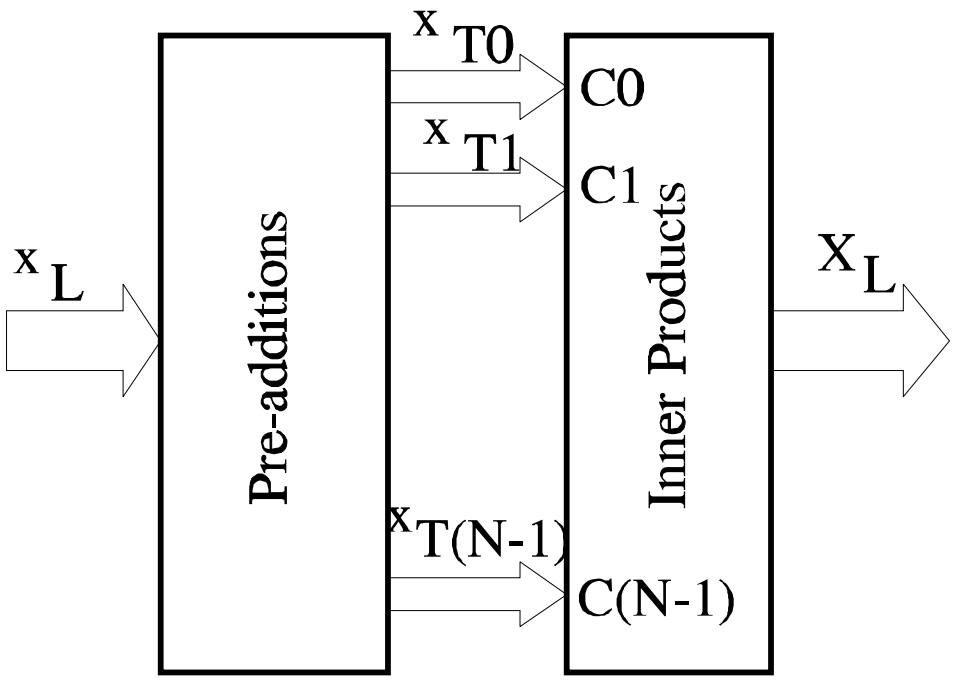
$$X_L = [F0]x_L + [F1]x_L + ... + [F(N-1)]x_L = \sum_{i=0}^{N-1} [Fi]\ x_L = \sum_{i=0}^{N-1} Ci\ [Ti]\ x_L$$

Because of the odd even property of the 2-D DCT

$$X_L^{EVEN} = \sum_{i=0}^{N/2-1} C(2i)\ \{\ [T(2i)]\ x_L\ \}$$

$$X_L^{ODD} = \sum_{i=0}^{N/2-1} C(2i+1)\ \{\ [T(2i+1)]\ x_L\ \}$$

The computational steps of the proposed algorithm



The preaddition phase is consists of 5 levels of butterfly operations

$$X_L = [E][D][C][B][A]x_L$$

If $[I_{N/2}]$ and $[I_{N/2}^{*}]$ are the normal and opposite identity matrices then the butterfly matrix

$$[L_N] = \begin{vmatrix} [I_{N/2}] & [I_{N/2}^{*}] \\ [I_{N/2}^{*}] & -[I_{N/2}] \end{vmatrix}$$

$$X_B = [A]\, x_L \quad ; \quad X_C = [B]\, X_B \quad ; \quad X_D = [C]\, X_C$$

$$[A] = [L_{64}]$$

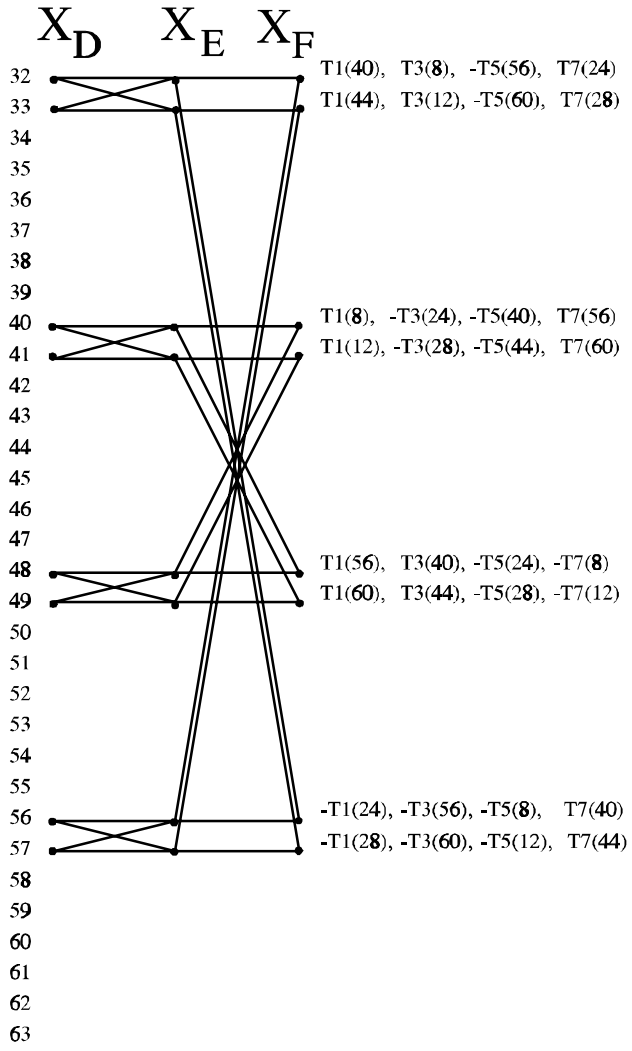
$$[B] = diag \ \{ \ [L_8],[L_8],[L_8],[L_8],[L_8],[L_8],[L_8],[L_8] \ \}$$

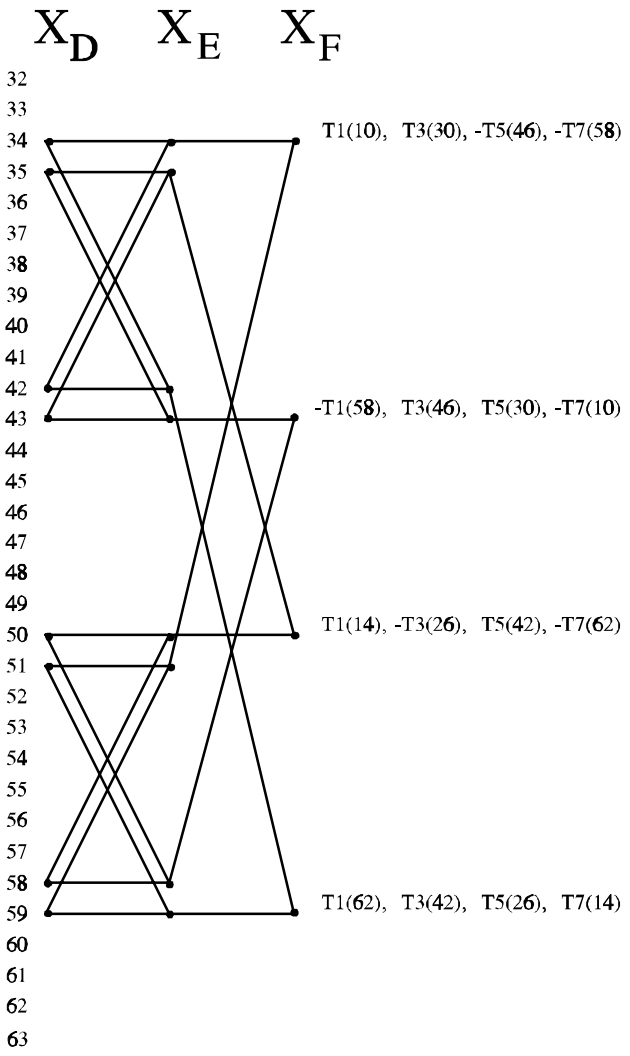
$$[C] = diag \ \{ \ [L_4],[L_4],[L_4],[L_4],[L_4],[L_4],[L_4],[L_4],[L_4],[L_4],[L_4],[L_4],[L_4],[L_4],[L_4],[L_4] \ \}$$

The number of arithmetic operations in the preaddition phase is proportional with N^2

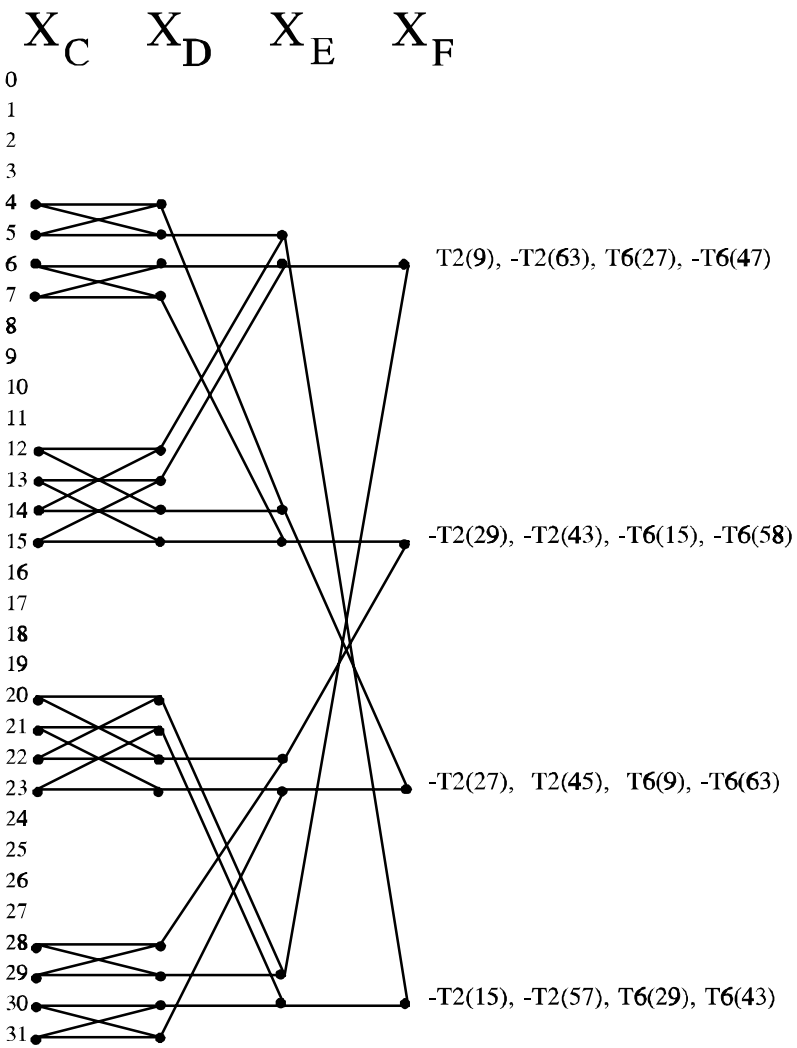
$$C_{PA} \cong N^2 \cdot \log_2 N^2$$

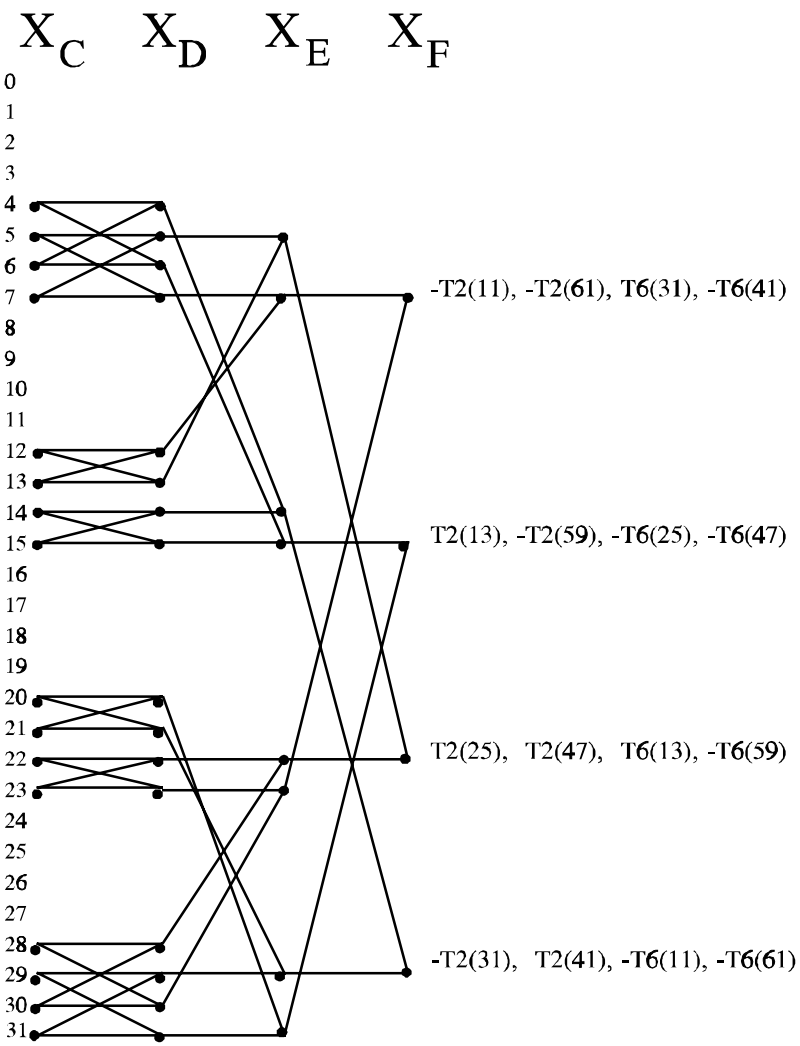
Example signal flowgraphs of some of the even components (2 of 6)





Example signal flowgraphs of some of the odd components (2 of 5)





INTERNAL STRUCTURE OF THE INNER PRODUCT PROCESSORS

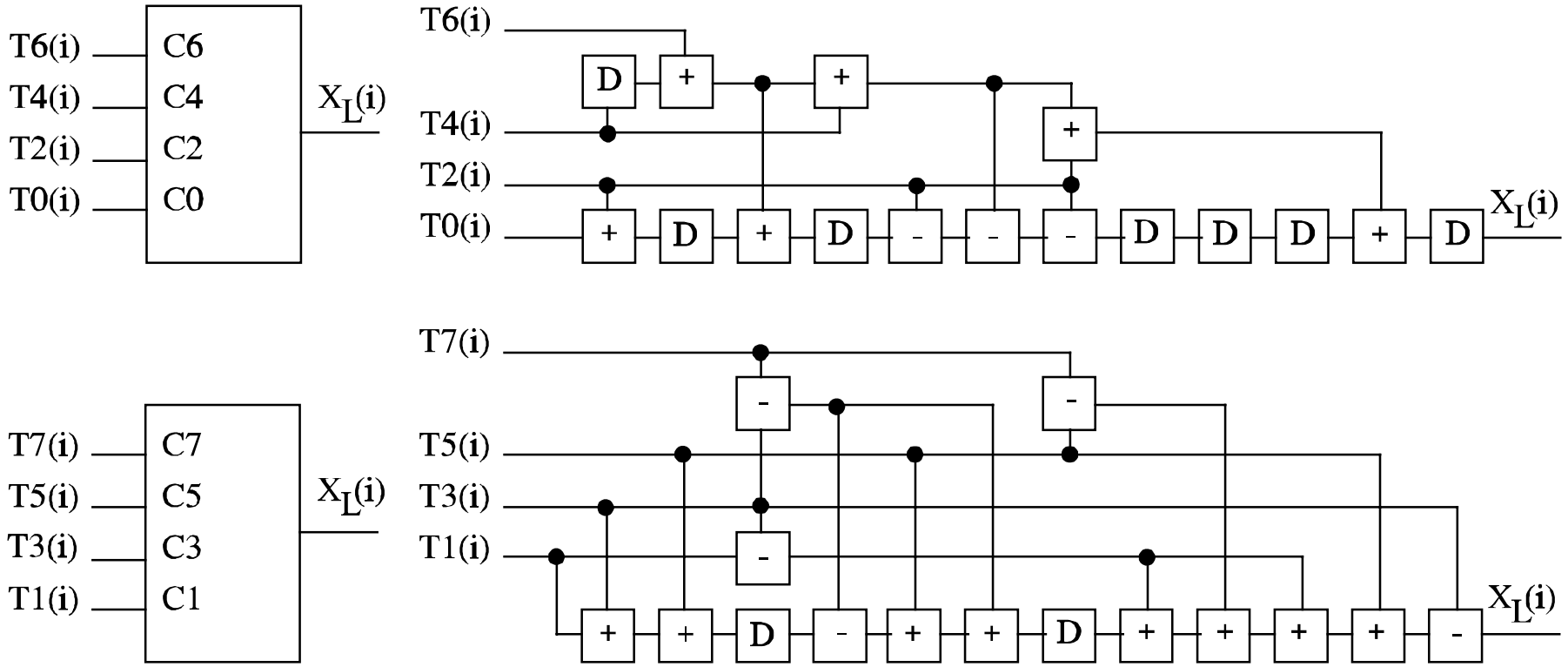
Dedicated, merged serial/parallel multiplier modules for the fixed Ci values

CSD number representation and bit level optimization to reduce arithmetic complexity

$$
\begin{aligned}
C0 &= 1_{10} = 1.0000000000000000_{CSD} \\
C1 &= 0.9808_{10} = 1.0000\,0\,{-1}\,0\,{-1}\,0000\,1\,01_{CSD} \\
C2 &= 0.9239_{10} = 1.000\,{-1}\,0\,{-1}\,00\,1\,0000_{CSD} \\
C3 &= 0.8315_{10} = 1.0\,{-1}\,0\,1\,0\,1\,0\,1\,00\,{-1}\,00\,{-1}_{CSD} \\
C4 &= 0.7071_{10} = 1.0\,{-1}\,0\,{-1}\,0\,1\,0\,1\,0000\,1_{CSD} \\
C5 &= 0.5556_{10} = 0.1\,00\,1\,00\,{-1}\,00\,1\,00\,{-1}\,0_{CSD} \\
C6 &= 0.3827_{10} = 0.1\,0\,{-1}\,000\,1\,000\,1\,0_{CSD} \\
C7 &= 0.1951_{10} = 0.0\,1\,0\,{-1}\,00\,1\,000\,{-1}\,00_{CSD}
\end{aligned}
$$

Five inner product sets {C0}, {C0, C4}, {C2, C6}, {C0, C2, C4, C6}, {C1, C3, C5, C7}

The signal flow graph of the two 4 input inner product processors

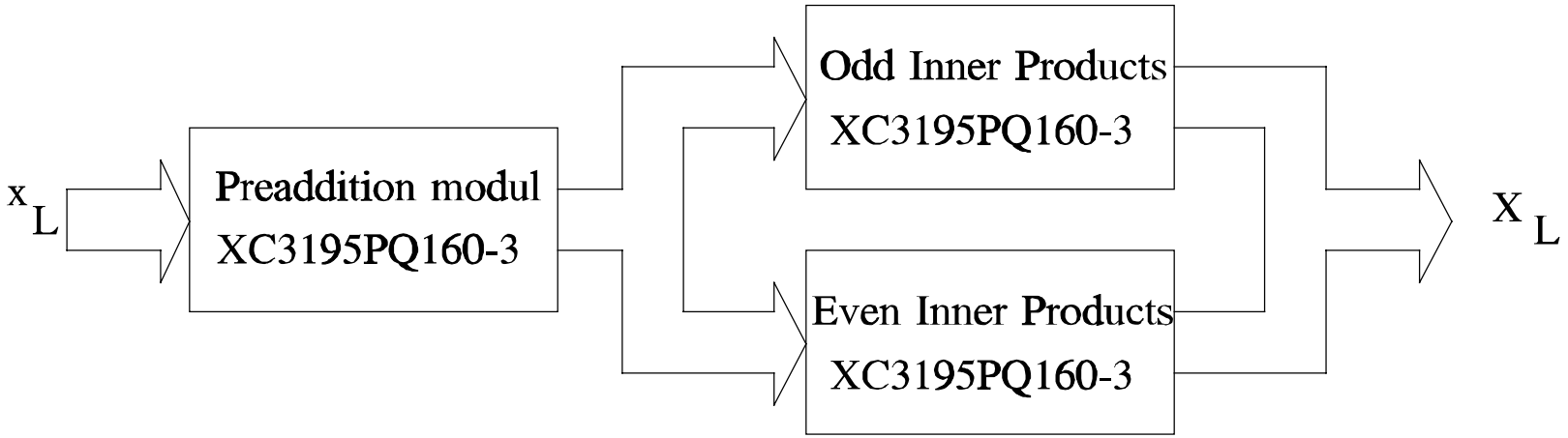


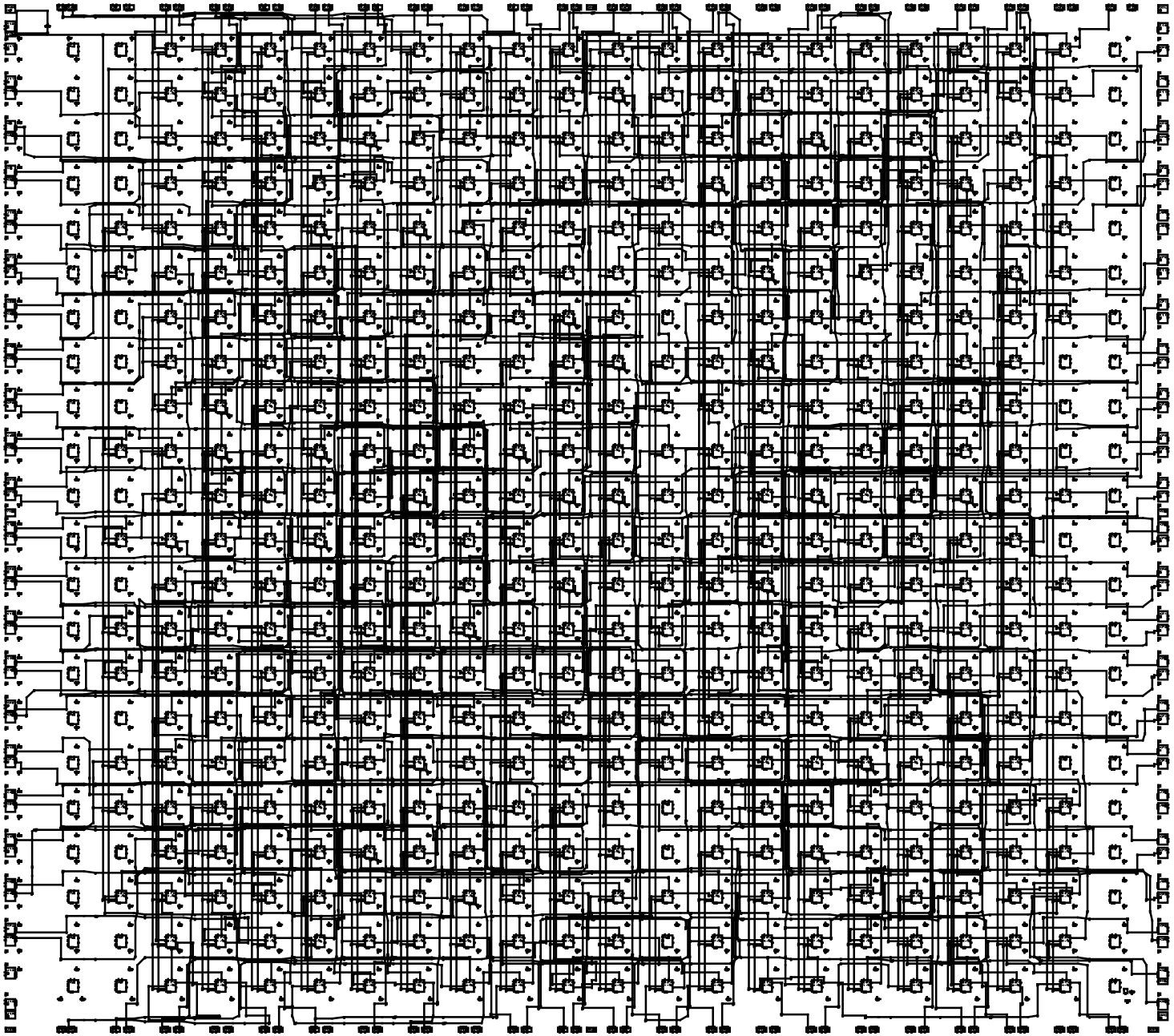
LSB first serial operation, 12 bit constant representation

Total number of logic resources

	Preadd	C1..C7 IPPs	C0 delay	C0-C4 IPPs	C2-C6 IPPs	C0..C6 IPPs	Total
+/-	418	416	0	20	48	144	1046
Del	0	64	48	28	48	112	300

Example implementation on 3 Xilinx XC3195PQ160-3 devices





Preaddition module

5 levels of butterflies

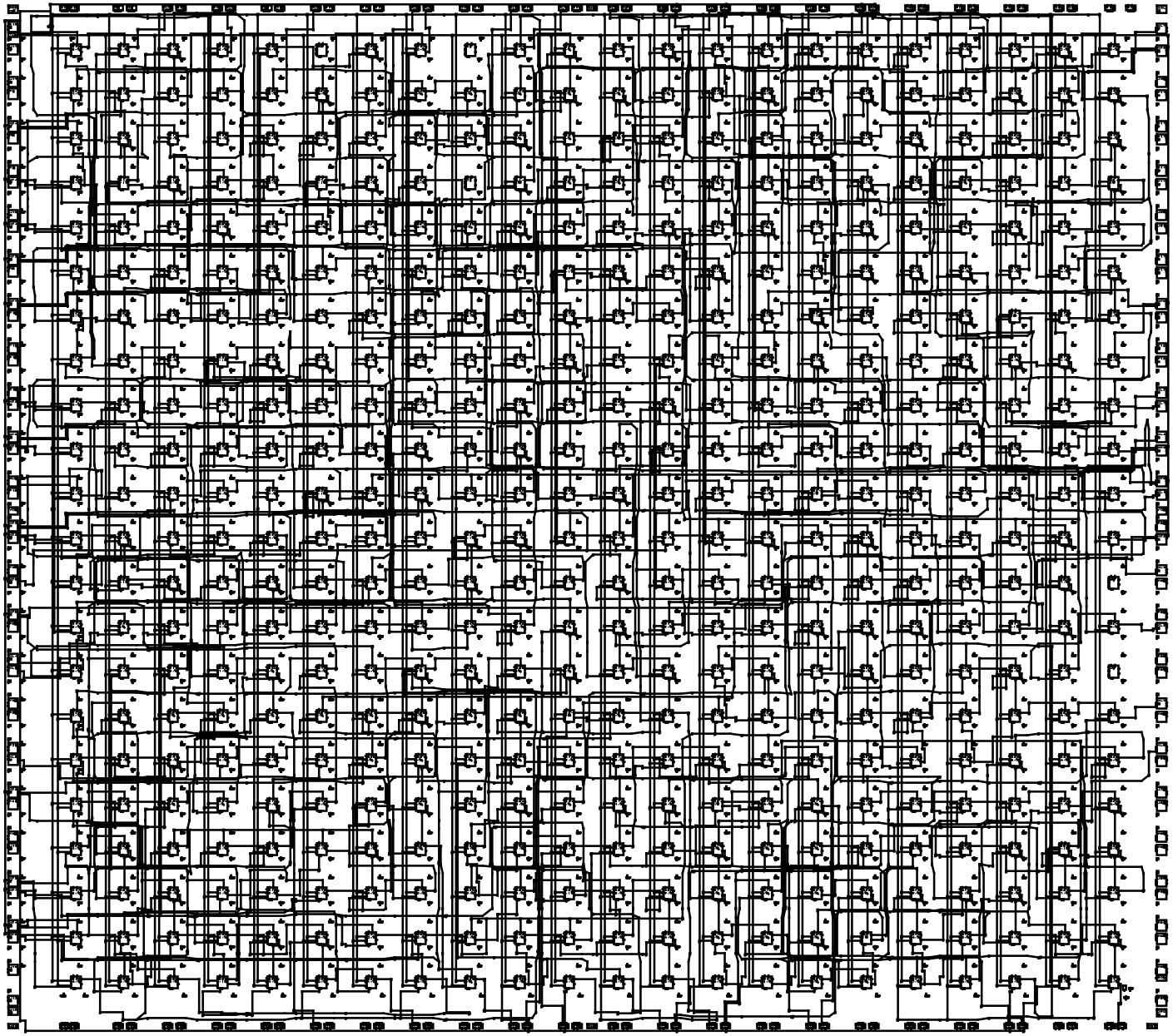
Device: XC3195PQ160-3

Utilization:418/484 CLB

132/138 IOB

Maximum clock frequency

>30 MHz



Odd Inner Product module

32 4 input multiplier

Device: XC3195PQ160-3

Utilization:479/484 CLB

66/138 IOB

Maximum clock frequency

>30 MHz

CONCLUSIONS

Direct 2-D DCT algorithm,

Two independent computation step

Concurrent parallel architecture

Serial LSB first arithmetic

Dedicated inner product processors

FPGA implementation